SONA COLLEGE OF TECHNOLOGY

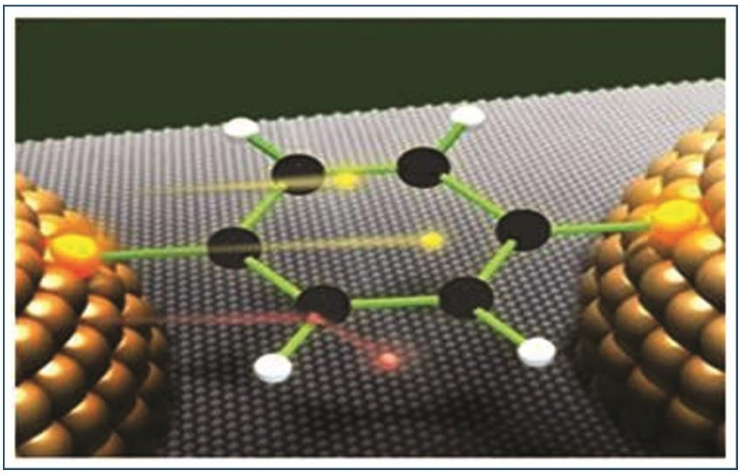
Learning is a Celebration!

| An Autonomous Institution |

Department of Electronics and Communication Engineering

MICROELECTRONICS TO NANOELECTRONICS

2022-23



Junction Main Road
Suramangalam (PO)
Salem-636 005. TN. India
www.sonatech.ac.in

Editorial Head

Dr.R.S.Sabeenian,
Professor &Head, Dept of ECE,
Head R&D Sona SIPRO

Editorial Members

Dr.K.R.Kavitha Professor		Mr.J.Harirajkumar Associate Professor	
Ms.M.Susaritha Assistant Professor		Magazine co-ordinator Dr.K.Manju Assistant Professor	

FIND YOUR PRODUCT USING WEB APPLICATION

MUGILAN RS, NAVEEN SIVAA S

ABSTRACT

This project focuses on the development of a web application that facilitates the connection between users and vendors for posting and fulfilling product requests. The application is built using HTML, CSS, PHP, and MySQL as the backend database. Users and vendors have separate login systems to ensure secure access. Users can submit their product requests through the application, while vendors can browse and respond to these requests. The project provides an overview of the system architecture, emphasizing the client-server model. It highlights the significance of bridging the gap between users and vendors by offering a platform that streamlines communication and transactions. The web application aims to enhance user experience, foster efficient connections, and provide a user-friendly interface for seamless interaction between users and vendors.

1.INTRODUCTION

The rise of online shopping has significantly transformed the retail industry, providing consumers with unparalleled convenience, accessibility, and an extensive range of products. This transformation has been further accelerated by the advent of web development technologies and the emergence of mobile shopping apps. In this project will explore the profound impact of web development on the shopping industry and the role of online shopping apps in revolutionizing the way in this project. Online shopping has witnessed a remarkable evolution over the years, from the early days of basic e-commerce

websites to the advanced mobile shopping apps in this we have today. This evolution has been driven by the increasing reliance on web development technologies, which have enabled businesses to create seamless and user-friendly platforms for customers to browse, select, and purchase products. Web development plays a crucial role in the creation of online shopping apps by providing the necessary tools and frameworks to design and develop highly functional and visually appealing interfaces.

With the advent of responsive web design, shopping apps can adapt to different screen sizes and devices, ensuring a consistent and optimized experience for users across various platforms. One of the significant advancements in web development for shopping apps is the development of native and hybrid apps. Native apps are specifically designed for a particular operating system (such as iOS or Android) and provide superior performance and access to device-specific features. On the other hand, hybrid apps offer the advantage of cross-platform compatibility while still delivering a native-like experience. Both approaches have revolutionized the mobile shopping experience by allowing users to access their favourite stores and products directly from their smartphones.

Design is a critical aspect of web development for shopping apps. User Experience (UX) and User Interface (UI) design principles are employed to create intuitive and visually appealing interfaces that enhance the overall shopping experience. Seamless navigation, clear product information, and aesthetically pleasing layouts are crucial elements that contribute to the success of an online shopping app. Moreover, web development has enabled the integration of essential features and functionalities in shopping apps. User registration and authentication ensure secure access to user accounts and personalized experiences. Product catalogue management ensures efficient organization and presentation of products, including detailed descriptions, images, and pricing information. Streamlined shopping cart and checkout processes, along with

secure payment gateways, facilitate convenient and secure transactions. Additionally, order tracking and notifications keep users informed about the status of their purchases, providing a sense of reassurance and transparency.

Web development has also played a pivotal role in enhancing the shopping experience through personalization and recommendation systems. By leveraging user data, shopping apps can provide personalized product recommendations based on individual preferences and browsing behaviour, offering a tailored shopping experience. The integration of augmented reality (AR) technology has further enhanced the user experience by allowing customers to visualize products in their real environment or virtually try them on, enabling informed purchasing decisions. Security and trust are fundamental aspects of online shopping apps, and web development has facilitated the implementation of robust security measures. Secure payment systems, encryption technologies, and adherence to industry standards ensure the protection of user data and secure financial transactions. Transparent return policies, dispute resolution mechanisms, and customer reviews contribute to building trust and credibility among app users. web development has been instrumental in the transformation of the shopping industry, enabling the creation of mobile shopping apps that offer unparalleled convenience, personalization, and security. As technology continues to evolve, web development will continue to shape the future of online shopping, providing innovative solutions and optimizing the shopping experience for consumers worldwide.

2.EXISTING METHOD

In the realm of e-grocery web applications, various existing methods are employed for both cash on delivery (COD) and online payments. These methods play a vital role in ensuring smooth and secure transactions between customers and e-grocery platforms. Let's explore these methods in more detail. E-grocery web apps strive to provide a range of payment options to cater to the diverse

preferences and needs of their customers. By offering both cash on delivery and online payment methods, these platforms ensure flexibility and convenience for customers while maintaining the security and trust necessary for successful transactions. The availability and adoption of specific payment methods may vary depending on the region, customer demographics, and the e-grocery platform's partnerships with payment service providers.

2.1 CASH ON DELIVERY (COD)

Cash on Delivery is a popular payment method in e-grocery web apps. It allows customers to place orders online and make the payment in cash upon the delivery of their groceries. This method is particularly favoured by customers who prefer not to share their financial information online or may not have access to digital payment options. With COD, customers have the convenience of receiving and inspecting their groceries before making the payment. It stills lacks in trust and confidence in the purchase process and is widely used in regions where digital payment adoption is still developing.

2.2 ONLINE PAYMENTS

E-grocery web apps also offer various online payment methods for customers who prefer digital transactions. Credit and debit card payments are commonly supported, where customers can securely enter their card details during the checkout process. Digital wallet options, such as PayPal, Google Pay, or Apple Pay, are often integrated into e-grocery platforms, providing users with a convenient and secure way to make payments using their stored payment information. Online banking transfers are another popular option, allowing customers to transfer funds directly from their bank accounts to the e-grocery platform.

2.3 MOBILE PAYMENT APPS

In addition to traditional online payment methods, many e-grocery web apps have incorporated mobile payment apps into their platforms. These apps, like Paytm, Alipay, or WeChat Pay, allow customers to make payments using their smartphones. Customers can link their bank accounts or cards to the mobile payment apps, providing a seamless and convenient way to complete transactions. Mobile payment apps are particularly popular in regions where smartphone usage is widespread and customers prefer the convenience of making payments on their mobile devices.

3.PROPOSED METHOD

3.1 STUDY AREA: DISINTERMEDIATION

Online shopping apps are revolutionizing the shopping experience for offline shoppers by providing them with real-time visibility into their products' whereabouts. Through features like order tracking and delivery updates, customers can stay informed about the status of their purchases. This empowers offline shoppers with information and alleviates anxieties regarding delivery delays or uncertainties. Disintermediation in online shopping apps also promotes transparency by enabling customers to access detailed information about vendors. This includes vendor profiles, customer ratings and reviews, product sourcing details, and contact information. By having direct access to this information, customers can make more informed decisions about their purchases, fostering trust and accountability in the online marketplace.

3.2 TOOLS USED

Web development relies on a range of tools and technologies to create dynamic and interactive websites and web applications. In this section, in this project will explore the key tools used in web development, specifically focusing on HTML, CSS, PHP, MySQL, Wamp Server, and phpMyAdmin shows in Table 4.1. These

tools form the backbone of the development process, enabling developers to design, code, and manage the functionality and data of web applications.

Parameter	User Experience	Significance
HTML	Determines the structure of web pages	Essential for creating the layout and organizing content
CSS	Defines the visual appearance	Crucial for styling elements, improving aesthetics, and branding
PHP	Enables server-side scripting	Allows dynamic content generation, form processing, and database interaction
MySQL	Manages relational databases	Facilitates efficient storage and retrieval of data
WAMP	Server Provides a local development environment	Simplifies the setup and testing of the web application locally
phpMyAdmin	Offers a web-based database management tool	Streamlines the administration of the MySQL database

Table 4.1 Tools Used

define the elements on a webpage, such as headings, paragraphs, images, links, and forms. Developers use HTML to create the structure and semantic meaning of a webpage, allowing browsers to interpret and display the content correctly.

3.2.2 CSS

CSS is used to style and enhance the visual presentation of web pages. It works alongside HTML by providing rules and declarations that define how elements should be displayed. CSS controls various aspects of web design, including

colours, typography, layout, and responsiveness. By separating the content (HTML) from the presentation (CSS), developers can create visually appealing and consistent web pages.

3.2.3 PHP

PHP is a server-side scripting language used for developing dynamic web pages and web applications. It is embedded within HTML code and executed on the server before being sent to the client's browser. PHP allows developers to create interactive features, handle form data, connect to databases, and perform various server-side tasks. It provides extensive functionality and flexibility, making it a popular choice for web development.

3.2.4 MySQL

MySQL is a popular open-source relational database management system. It is widely used in web development to store, manage, and retrieve data. MySQL offers a robust and efficient platform for handling structured data in web applications. Developers can utilize PHP to interact with MySQL databases, perform queries, insert, update, and delete data, and ensure data integrity and security.

3.2.5 WAMP SERVER

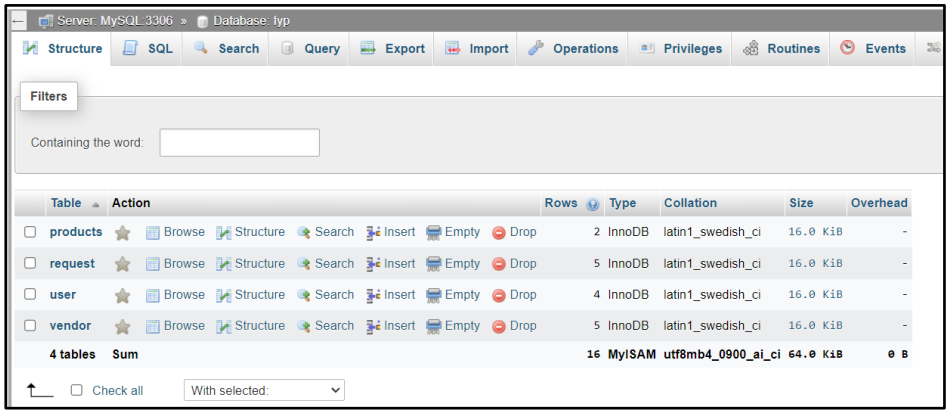
Wamp Server is a software stack that provides a local development environment for web applications. It includes the Apache web server, PHP interpreter, and MySQL database, bundled together in a single installation package. Wamp Server allows developers to set up a local server environment on their computer, enabling them to develop and test web applications offline. It provides a convenient and efficient way to build and debug applications before deploying them to a live server.

3.2.6 PHPMYADMIN

phpMyAdmin is a web-based graphical interface used for managing MySQL databases. It allows developers to interact with databases through a user-friendly interface, simplifying tasks such as creating databases, tables, and executing SQL queries. phpMyAdmin provides tools for importing and exporting data, managing user permissions, and optimizing database performance. It is an essential tool for developers working with MySQL databases in web development projects.

3.3 DATABASE MANAGEMENT

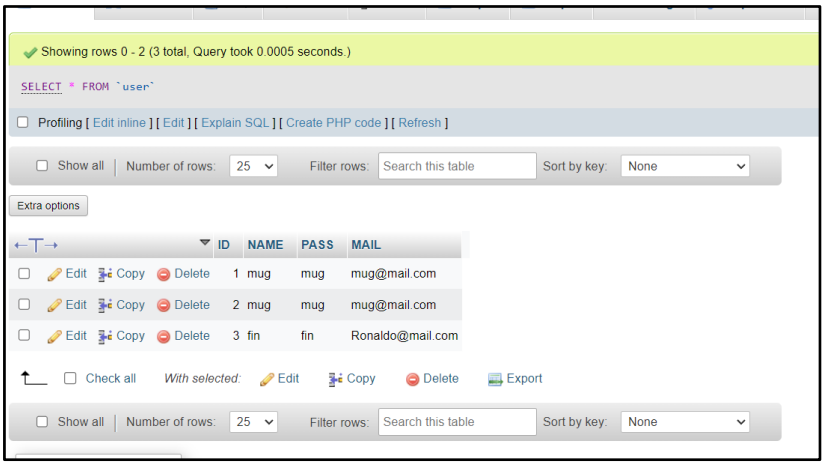
Effective database management is essential for ensuring data accuracy, consistency, and security. By utilizing MySQL and appropriate database design principles, developers can create a robust and scalable system that efficiently handles customer, vendor, request, and billing data, contributing to a seamless and reliable user experience within the web application. In the context of web development, effective database management is crucial for storing, organizing, and retrieving data. MySQL, being a popular relational database management system shown in Fig 4.1 provides a robust platform for managing data in web applications. In this section, in this project will focus on the management of four key tables: Customers, Vendors, Requests, and Bills, where the primary keys are assigned as user IDs.



Database

3.3.1 CUSTOMERS DATA TABLE

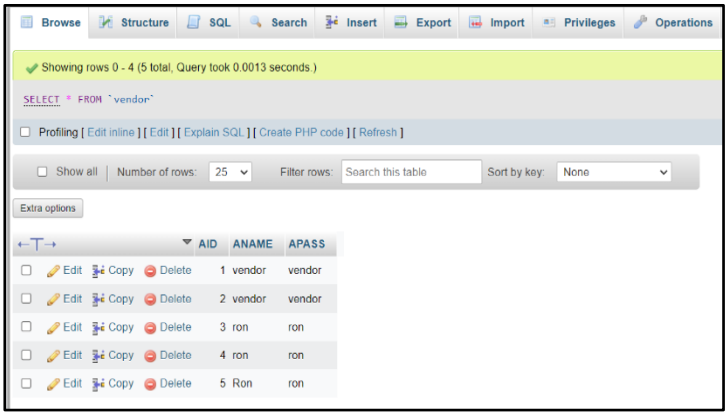
The Customers table serves as a central repository for storing information about individual customers. Each customer is assigned a unique user ID, which acts as the primary key in the table as shown in Fig 4.2. The table includes columns such as name, contact details, shipping address, and any other relevant customer-specific data. The primary key ensures the uniqueness and efficient retrieval of customer records.



Customer Database

3.3.2 VENDORS DATA TABLE

The Vendors table contains information about various vendors associated with the web application. Similar to the Customers table, each vendor is assigned a unique user ID as the primary key as shown in Fig 3.3. The table includes columns for vendor details, such as name, contact information, location, and other relevant vendor-specific data. The primary key facilitates easy identification and retrieval of vendor records.



Vendor Database

3.3.3 REQUESTS DATA TABLE:

The Requests table tracks the product requests made by customers. Each request is assigned a unique request ID, acting as the primary key. The table includes columns for customer ID, vendor ID, requested product details, quantity, status, and timestamps. The primary key ensures the efficient management and retrieval of specific request information, enabling seamless tracking and processing.

3.3.4 BILLS DATA TABLE:

The Bills table stores the billing information related to customer purchases. Each bill is assigned a unique bill ID as the primary key. The table includes columns for customer ID, vendor ID, product details, quantity, pricing, payment status, and timestamps. The primary key enables efficient retrieval of specific billing details and facilitates seamless management of customer transactions.

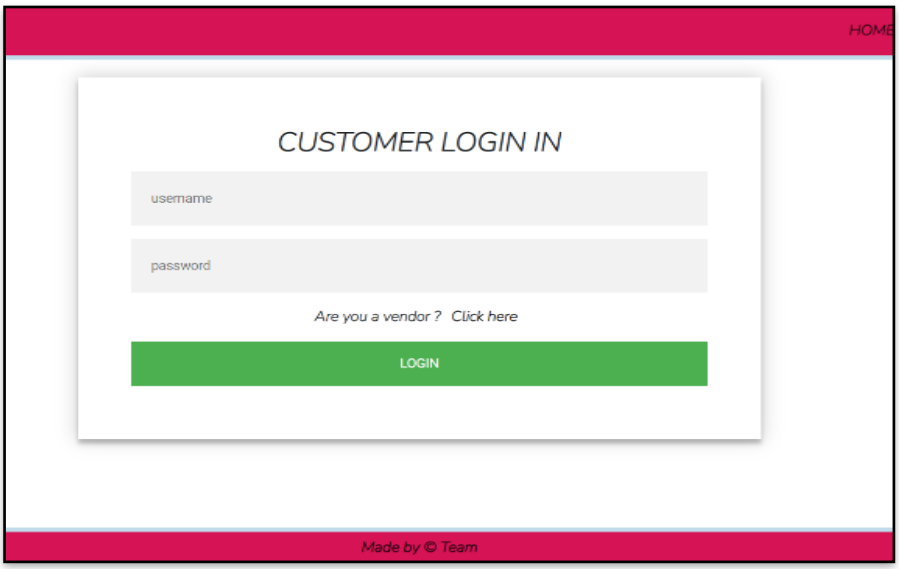
4.METHODOLOGY

4.1 LOGIN SYSTEMS SEGMENTATIONS

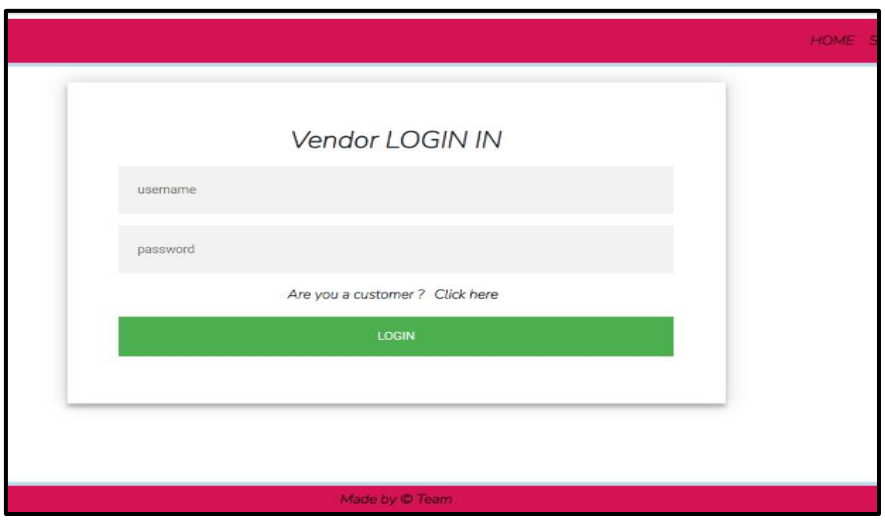
The login system implemented for customers in the web application allows them to post their product requests and search for specific items in a table that includes product images and prices. Customers have the flexibility to search for products using various parameters such as product name, price, or tags. This feature enhances the user experience by enabling customers to quickly find the products they are looking for as shown in Fig.

Additionally, vendors have access to a dedicated section where they can view the requests submitted by customers as shown in Fig. The system provides

vendors with essential details such as the time of the request and the specific products that customers are seeking. This functionality empowers vendors to efficiently manage and respond to customer requests, ensuring timely and accurate communication. By implementing this login system, the web application creates a streamlined platform that bridges the gap between customers and vendors. Customers can easily express their product needs, while vendors can effectively track and address those requests. This seamless interaction between customers and vendors fosters a dynamic and efficient marketplace where transactions can take place smoothly.



Customer Login

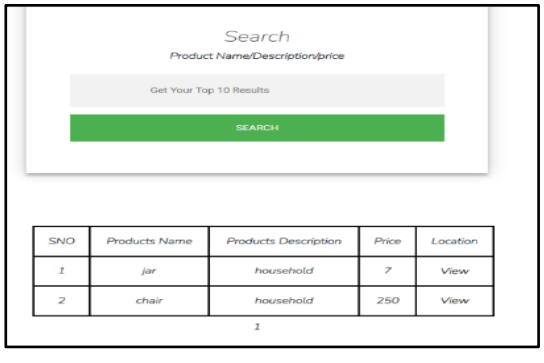


Vendor Login

4.2 ENHANCED USER EXPERIENCE:

The web application incorporates tabular representation for displaying search results, offering users a visually organized and easily understandable view of the products. By presenting the results in a tabular format, users can quickly scan through the information, including product images and prices, in a structured manner. This improves the overall user experience and facilitates efficient decision-making as shown in Fig 5.3. Moreover, the login system allows users, both customers and vendors, to change their passwords securely. This feature ensures that users have control over their account security and can update their passwords periodically to maintain confidentiality and protect their personal information.

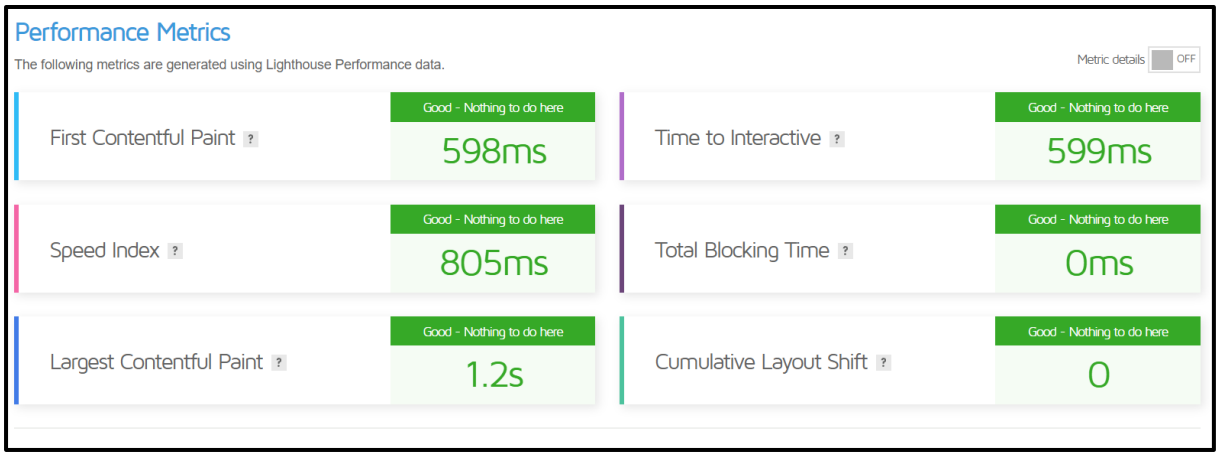
Additionally, vendors have the ability to upload images of their products. This functionality allows vendors to showcase their offerings visually, enabling customers to get a better understanding of the products they are interested in. By uploading images, vendors can effectively market their products and attract potential buyers, leading to increased sales and customer engagement. The inclusion of password change functionality and product image upload feature adds value to the web application, enhancing both security and user experience. Users can confidently manage their account credentials, ensuring the safety of their data. Vendors can showcase their products more effectively, providing customers with a richer and more engaging browsing experience.



Search View

5.RESULTS & DISCUSSION

`In this section, analyzation of the project and present the results obtained from the implementation of the web application. The analysis will focus on various aspects, including user engagement, functionality performance, and feedback received during the testing phase. The results will highlight the effectiveness of the application in meeting its objectives and providing a seamless user experience as shown in Fig .



Performance Metrics

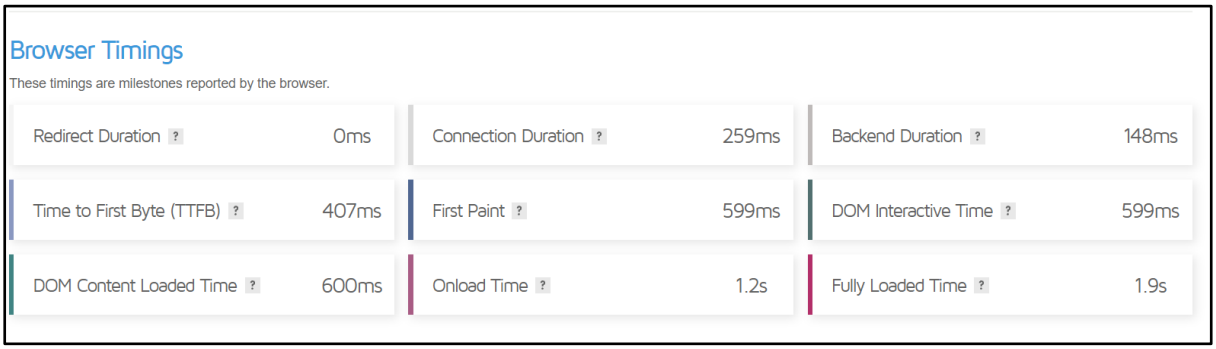
By analysing these performance metrics, developers can identify potential bottlenecks and areas for optimization. This could be used to fine-tune the code, optimize database queries, and leverage caching techniques to improve page load speed, reduce Total Blocking Time, and enhance overall user experience. Regular monitoring and performance testing are crucial to ensure that the application meets the expected performance standards and provides a seamless browsing experience for users as shown in Table. The parameters for each performance metric, such as First Contentful Paint, Time to Interactive, Speed Index, Total

Blocking Time, Largest Contentful Paint, and Cumulative Layout Shift. The "Time Taken" column indicates the measured time for each metric, while the "Normal Range" column specifies the recommended normal range for optimal performance. It is important to note that the values provided in the "Normal Range" column are general guidelines and may vary depending on specific project requirements and performance standards.

Parameter	Time Taken	Normal Range
First Contentful Paint	494ms	< 1s
Time to Interactive	495ms	< 5s
Speed Index	706ms	< 1,000ms
Total Blocking Time	0ms	< 50ms
Largest Contentful Paint	1.1s	< 2.5s
Cumulative Layout Shift	0	< 0.1

Performance Metrics

Monitoring these metrics and striving to keep them within the normal range can help ensure a fast and responsive web application.



Browser Timings

The performance analysis of the web application revealed promising results. The redirect duration of 0ms indicates an efficient implementation, eliminating any unnecessary redirects and optimizing the user's browsing experience. The connection duration of 259ms reflects a reasonably fast

establishment of a connection with the web server, ensuring a smooth and responsive user experience. With a backend duration of 148ms, the server efficiently processes the requests, resulting in quick response times. The time to first byte (TTFB) of 407ms indicates the duration between the request and the first bit of data being received, reflecting a relatively speedy server response. The first paint occurring at 599ms signifies that the initial content is rendered on the screen, ensuring a visually engaging user interface. The DOM interactive time, DOM content loaded time, and onload time all occurring within a close timeframe of 599ms to 1.2s demonstrate the web application's responsiveness, allowing users to interact with the content swiftly. The fully loaded time of 1.9s indicates that the entire web page, including images, scripts, and other resources, is loaded successfully. Overall, these performance metrics indicate an efficient and optimized web application, offering users a seamless and satisfying browsing experience.

6.CONCLUSION

The development and implementation of the web application for online shopping have proven to be a significant advancement in the realm of e-commerce. The online shopping app has provided customers with a convenient and accessible way to post their product requests and search for specific items. With the ability to search by name, price, or tag, customers can quickly find the products they desire, enhancing their overall shopping experience. The tabular representation of search results further improves usability, allowing users to easily compare prices and view product images for informed decision-making. Furthermore, the login system implemented for customers and vendors has played a crucial role in enhancing security and personalization. Customers can securely log in, manage their account information, and change passwords as needed. Vendors, on the other hand, can access a dedicated section to view customer requests, enabling efficient tracking and response.

DESIGN AND CHARACTERIZATION OF PARALLEL PREFIX ADDERS

JAISURYA K, PRASHANTH KUMARAN P

ABSTRACT

The Project is to analyze the performance comparison of different types of carry-tree adders, namely the Kogge-Stone, Brent-Kung, and Han-Carlson, with the conventional Ripple Carry Adder (RCA) and Carry Skip Adder (CSA) on a Altera Development and Education Board. Based on parameter such as Delay, Power Consumption, Better Speed performance, Overall, This highlights the importance of considering the specific requirements and constraints of FPGA implementations when choosing the appropriate adder design. While carry-tree adders may offer superior performance in arithmetic operation, and we can use for some of the applications like Digital Signal Processors, Cryptography, Image video processing and so on.

1. INTRODUCTION

The binary adder is the critical element in most digital circuit designs including digital signal processors (DSP) and microprocessor data path units. As such, extensive research continues to be focused on improving the power- delay performance of the adder. In VLSI implementations, Parallel Prefix adders are known to have the best performance. Reconfigurable logic such as Field Programmable Gate Arrays (FPGAs) has been gaining in popularity in recent years because it offers improved performance in terms of speed and power over DSPbased and microprocessor-based solutions for many practical designs

involving mobile DSP and telecommunications applications and a significant reduction in development time and cost over Application Specific Integrated Circuit (ASIC) designs. The power advantage is especially important with the growing popularity of mobile and portable electronics, which make extensive use of DSP functions. However, because of the structure of the configurable logic and routing resources in FPGAs, Parallel Prefix adders will have a different performance than VLSI implementations. In particular, most modern FPGAs employ a fast-carry chain which optimizes the carry path for the simple Ripple Carry Adder (RCA). In this Project, the practical issues involved in designing and implementing tree-based adders on FPGAs are described. An efficient testing strategy for evaluating the performance of these adders is discussed. Several tree-based adder structures are implemented and characterized on a FPGA and compared with the Ripple Carry Adder (RCA) and the Carry Skip Adder (CSA). Finally, some conclusions and suggestions for improving FPGA designs to enable better tree-based adder performance are given.

Parallel Prefix adders, also known as carry-tree adders, are high performance digital circuits designed to efficiently perform arithmetic addition operations. They are widely used in modern computer processors and other computational systems where fast and efficient arithmetic calculations are crucial. The traditional method of adding two binary numbers involves a series of carry propagation operations, where each bit addition depends on the carry generated from the previous bit addition. This sequential approach can limit the speed of addition operations, especially when dealing with large binary numbers. In contrast, Parallel Prefix adders utilize a parallel approach that allows multiple bit additions to be performed simultaneously. By exploiting the inherent parallelism in the addition process, Parallel Prefix adders can significantly improve the speed of addition operations. The key concept behind Parallel Prefix adders is the precomputation and distribution of carry signals across multiple stages. Instead of waiting for carry signals to propagate sequentially, carry lookahead logic is

employed to compute and distribute the carry signals in advance. This enables faster and more efficient addition operations. Parallel Prefix adders are typically designed using a hierarchical structure, consisting of multiple levels or stages. Each stage computes partial sums and carry signals based on the input bits. The carry signals are then distributed to the subsequent stages, enabling the computation of higher-order bits. The advantage of Parallel Prefix adders lies in their ability to perform addition operations in a constant number of time steps, regardless of the number of bits being added. This makes them highly scalable and suitable for a wide range of applications. Overall, Parallel Prefix adders offer a powerful solution for achieving high-speed arithmetic operations, making them a fundamental component in modern computing systems that demand efficient and fast calculations.

1.1. OBJECTIVE

In this Project, the main focus is on designing and evaluating various types of carry tree adders to determine their efficiency based on different parameters. The motivation behind this investigation is to overcome the time delay associated with traditional adders, such as Ripple Carry Adders, which have a linear carry propagation delay resulting in slower operation times and higher power consumption. By implementing different types of carry tree adders and conclude by the delay reports of the adders.

2.SYSTEM ANALYSIS

2.1 Existing System

The existing system was about the several types of Adders like(Kogge-Stone adder, Sparse Kogge adder, Spanning tree Adder, Carry Skip adder)and compares them with a Simple Ripple Carry Adder [1].They discussed that these adders are not effective as the Simple Ripple Carry Adder at low to moderate bit widths. This is not unexpected as the Xilinx FPGA has a fast carry chain which optimizes the performance of the ripple carry adder. we have indications that the carrytree adders eventually surpass the performance of the linear adder designs at

high bit-widths, expected to be in the 128 to 256 bit range. This is important for large adders used in precision arithmetic and cryptographic applications where the addition of numbers on the order of a thousand bits is not uncommon.

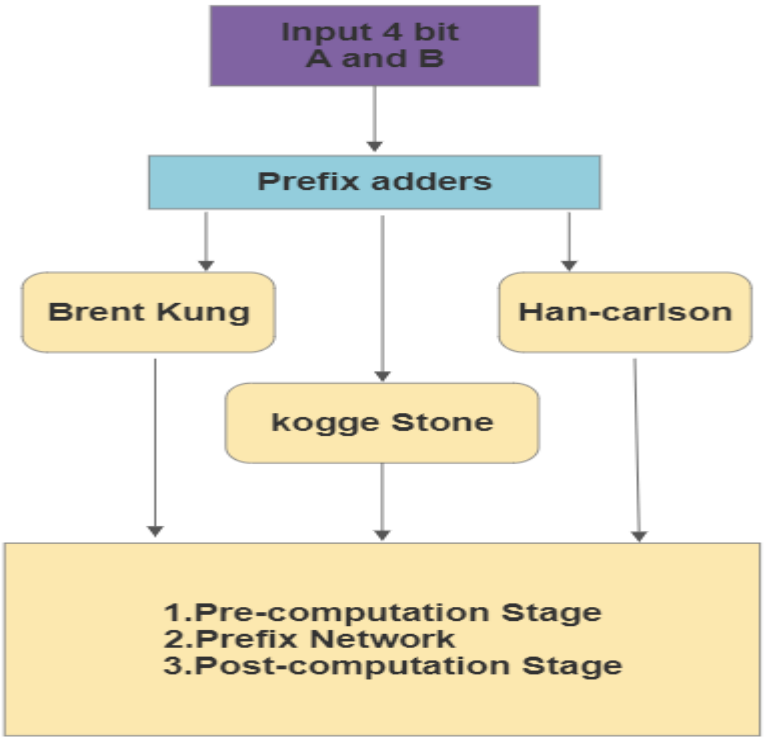
Because the adder is often the critical element which determines to a large part the cycle time and power dissipation for many Digital Signal Processing and cryptographical implementations, it would be worthwhile for future FPGA designs to include an optimized carry path to enable treebased adder designs to be optimized for place and routing. This would improve their performance similar to what is found for the RCA. We plan to explore possible FPGA architectures that could implement a “fast-tree chain” and investigate the possible trade-offs involved. The built-in redundancy of the Kogge-Stone carry-tree structure and its implications for fault tolerance in FPGA designs is being studied.

2.2 Proposed System

This Project is to design a Parallel Prefix adder with less delay, less area, and better speed performance. The focus of the project is to explore different types of Carry tree adders, including Kogge-Stone, Brent-Kung, and Han-Carlson , as well as comparing them with the simple Ripple Carry Adder (RCA) on an FPGA platform. The goal is to evaluate the performance of these adder designs in terms of their efficiency, area utilization, and speed of operation. By analyzing and comparing the results, the Project is to identify the most suitable Parallel Prefix adder design that exhibits improved characteristics compared to the traditional adders. The investigation will involve implementing the different adder designs in Verilog or another hardware description language, followed by synthesis and implementation on the FPGA platform. Delay, area and speed measurements will be performed using appropriate tools and techniques, such as timing analysis and logic synthesis. The outcome of this project will contribute to the understanding of the performance trade-offs and capabilities of various adder designs in FPGA-based systems. It will also provide insights into

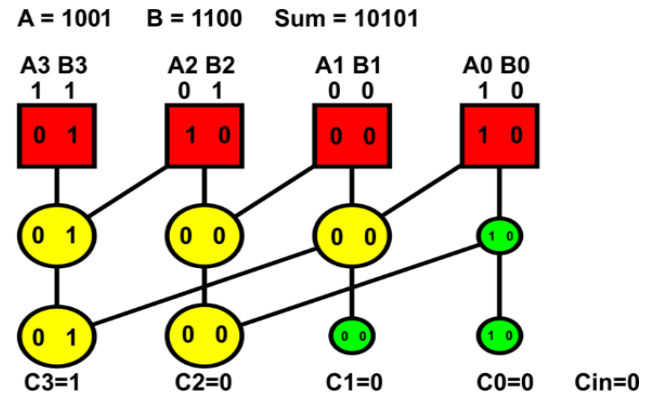
optimizing arithmetic operations for digital circuits, particularly in applications that require high-speed and efficient computations.

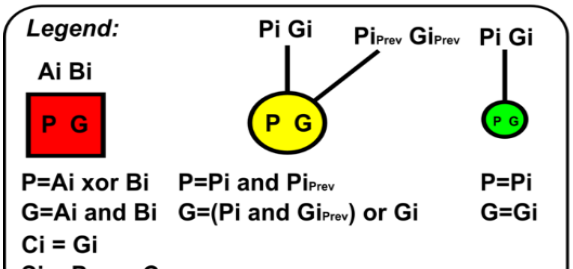
2.3 Proposed System Architecture



Block diagram of proposed system

3.1KOGGE STONE ADDER





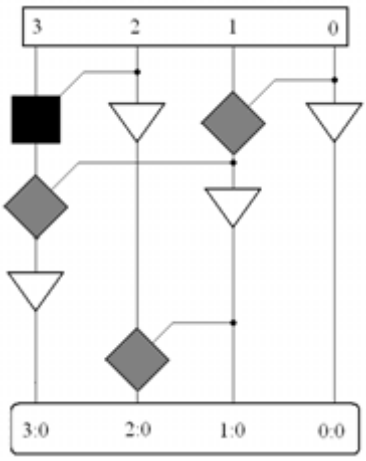
The Kogge-Stone adder is a fast parallel prefix adder used in digital circuits. It was developed by Peter Kogge and Harold Stone in the 1970s. This adder employs a tree-like structure of carry-lookahead units, allowing for the simultaneous calculation of carry bits. This parallel computation significantly enhances performance compared to ripple-carry adders. The Kogge-Stone adder finds extensive application in high-speed arithmetic circuits, including processors and digital signal processors, where it efficiently performs addition operations.

The Kogge–Stone adder takes more area to implement than the Brent–Kung adder, but has a lower fan-out at each stage, which increases performance for typical CMOS process nodes. However, wiring congestion is often a problem for Kogge–Stone adders. The Lynch–Swartzlander design is smaller, has lower fan-out, and does not suffer from wiring congestion; however to be used the process node must support Manchestor carry chain implementations. The general problem of optimizing parallel prefix adders is identical to the variable block size, multi level, Carry Skip Adder optimization problem, a solution of which is found in Thomas Lynch's thesis of 1996.

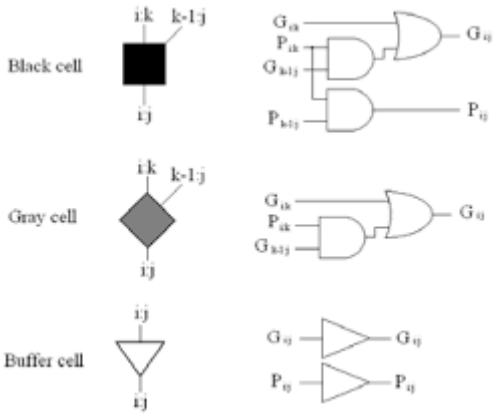
An example of a 4-bit Kogge–Stone adder is shown in the fig4.1. Each vertical stage produces a "propagate" and a "generate" bit, as shown. The culminating generate bits (the carries) are produced in the last stage (vertically), and these bits are XOR with the initial propagate after the input (the red boxes) to produce the sum bits. E.g., the first (least-significant) sum bit is calculated by XORing the propagate in the farthest-right red box (a "1") with the carry-in (a "0"), producing a "1". The second bit is calculated by XORing the propagate in second box from the right (a "0") with C0 (a "0"), producing a "0".

3.2 BRENT-KUNG ADDER

Brent-kung adder is used for high performance addition operation. The Brent-kung is the parallel prefix adder used to perform the addition operation . It is looking like tree structure to perform the arithmetic operation. The Brent-kung adder consists of black cells and gray cells. Each black cell consists of two AND gates and one OR gate . Each gray cell consists of only one AND gate.pi denotes propagate and it consists of only one AND gate given in equation



Brent-Kung adder Structure



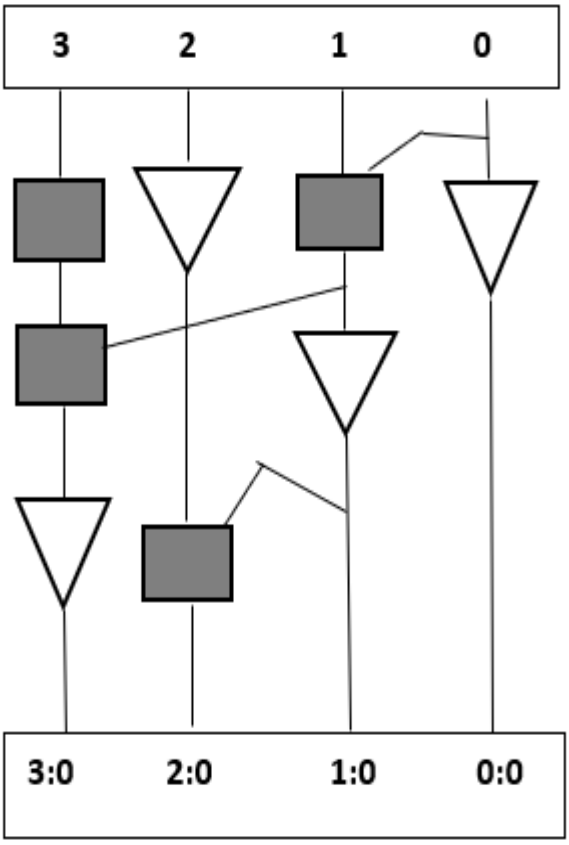
Brent-kung adder Blocks

1. gi denotes generate and it consists of one AND gate and OR gate given in equation
2. 2. pi= Ai XOR Bi -------- (1)
3. gi= Ai AND Bi ---------- (2)

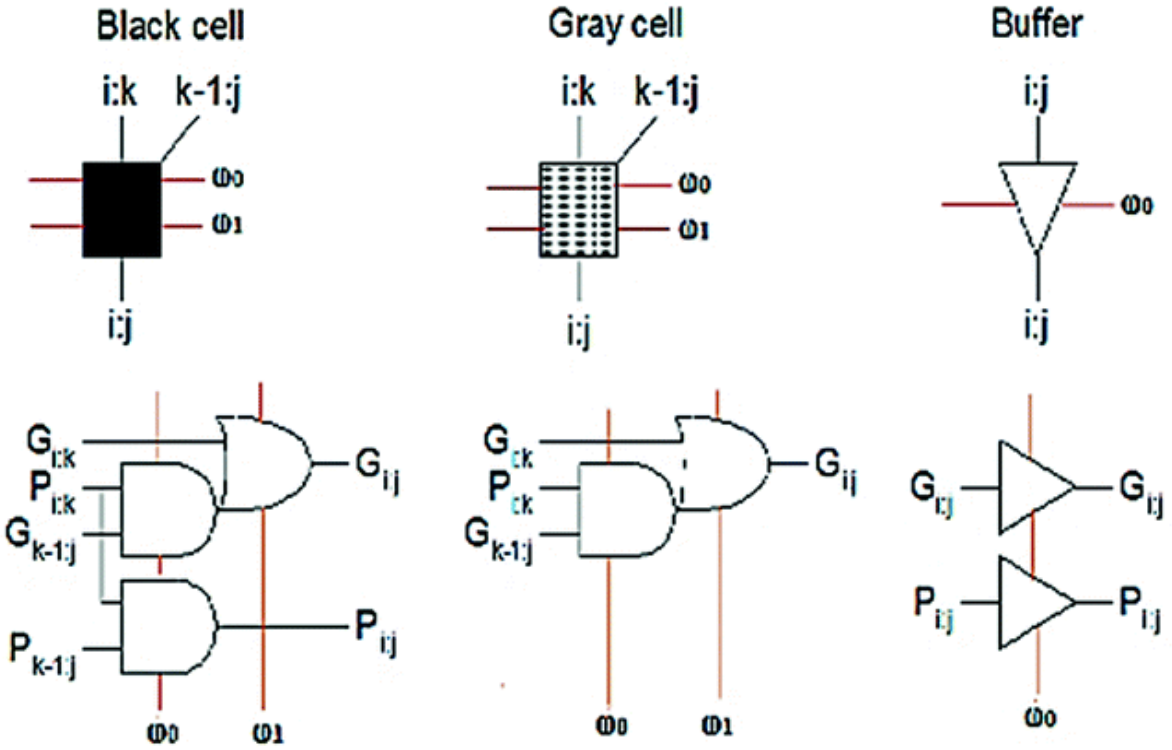
Gi denotes carry generate and it consists of one AND gate and OR gate given in equation 3 used for first black cell. he Brent-Kung adder divides the input

bits into groups and performs parallel computations to calculate the carry bits. It uses a tree structure where each node represents a carry-lookahead unit. At each level of the tree, the carry-lookahead units compute the carry bits based on the inputs from the previous level. The carry bits are propagated up the tree until they reach the root, where the final carry bit and the sum bits are generated. The Brent-Kung adder has a logarithmic depth, which means that the carry bits are calculated in parallel, resulting in improved performance compared to ripple-carry adders. It requires fewer carry-lookahead units compared to the Kogge-Stone adder, making it more area-efficient. However, the Brent-Kung adder has a longer critical path due to the increased depth of the tree structure, which may limit its maximum operating frequency.

3.3 HAN-CARLSON ADDER



Han-carlson adder Structure



Han-carlson adder blocks

Han-Carlson adder contains a good trade-off between fan out, number of logic levels and number of black cells. Because of this, Han-Carlson adder can achieve equal to speed execution admiration to Kogge-Stone adder, at lower power utilization and territory. In this manner it is fascinating to execute a speculative Han-Carlson adder. Moved by these reasons, we have generated a Han-Carlson speculative prefix-processing stage by removing the final rows of the Kogge-Stone part of the adder. As an example, Figure. 4.3 show the Han-Carlson adder in which the two Brent-Kung rows at the initial and toward the end of the graph are unaltered, while the last KoggeStone row is pruned. This yields a speculative stage with K=8=n/2.in general, one has K ==n/2p. where P is the quantity of pruned levels; the number of levels of the speculative HanCarlson stage lessens from 1+ log(n) to1+ log(k) (assuming that is a power of two).

The Han-Carlson adder is a variation of the Kogge-Stone adder that reduces the number of carry-lookahead units needed, resulting in improved performance. It achieves this reduction by grouping the bits into blocks and using a modified carry-lookahead unit at each block. The adder is divided into multiple stages, where each stage corresponds to a specific block of bits. Within each stage, the carrylookahead unit generates the carry-out for the corresponding block using a modified logic. The carry-out from each block is propagated to the next stage, allowing for parallel computation of carry bits. The final sum is obtained by combining the individual sum bits from each stage. The Han-Carlson adder provides a trade-off between the number of carry-lookahead units and the delay in calculating the carry bits. By reducing the number of carry-lookahead units, it reduces the complexity and improves the overall performance of the adder.

3.4 APPLICATIONS OF PARALLEL PREFIX ADDER

Processors: Parallel prefix adders are extensively used in the design of high-performance processors, including general-purpose CPUs, graphics processors, and specialized accelerators. They enable efficient arithmetic operations in these processors, contributing to faster overall performance.

Digital Signal Processors (DSPs): DSPs require fast and efficient arithmetic operations to process audio, video, and other realtime signals. Parallel prefix adders are used in DSP architectures to enable high-speed addition and accumulation operations required for various signal processing algorithms.

Cryptography: Cryptographic algorithms, such as encryption and decryption, involve intensive arithmetic computations on binary numbers. Parallel prefix adders are employed in cryptographic processors and hardware accelerators to speed up these calculations, enhancing the performance of secure communication systems.

Image and Video Processing: Parallel prefix adders play a vital role in image and video processing applications, such as image and video compression, filtering,

and transformation. These operations often involve arithmetic computations on large volumes of data, and the use of parallel prefix adders helps achieve real-time processing.

High-performance Computing (HPC): Parallel prefix adders are utilized in HPC systems for fast and efficient arithmetic operations in scientific simulations, data analytics, and numerical computations. They contribute to the overall computational performance of HPC architectures, enabling faster processing of complex algorithms.

FPGA and ASIC Designs: Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) employ parallel prefix adders due to their high-speed and areaefficient characteristics. They are used in various digital designs, including communication systems, network routers, and embedded systems.

3.5 ADVANTAGES

1. Speed: Parallel prefix adders can perform addition operations in parallel, allowing for faster computation compared to sequential adders. This is particularly beneficial in high-performance computing applications where speed is crucial.

2. Scalability: Parallel prefix adders can easily be scaled up to accommodate larger numbers of inputs without a significant increase in delay. This makes them suitable for applications that require addition of multiple numbers simultaneously, such as signal processing or graphics rendering.

3. Regularity: Parallel prefix adders have a regular structure that allows for efficient implementation and simplifies the design process. The regularity facilitates easier integration into larger circuits and enables better optimization and testing.

4. Low power consumption: Compared to other adder architectures, parallel prefix adders can offer lower power consumption due to their parallel nature. By

performing computations concurrently, the overall power consumption can be reduced, which is desirable in applications with limited power budgets, such as mobile devices or embedded systems.

5. Balanced delay: Parallel prefix adders distribute the carry propagation across multiple levels, resulting in a more balanced delay throughout the circuit. This balanced delay helps minimize critical path delays and improves overall performance.

6. Fault tolerance: The regular structure of parallel prefix adders enhances their fault tolerance. In the event of a fault in one of the adder stages, the impact on the overall performance is localized and can be mitigated more easily compared to other adder architectures.

Overall, parallel prefix adders offer improved speed, scalability, regularity, power efficiency, balanced delay, and fault tolerance, making them advantageous for various high-performance computing and digital system design applications.

4. HARDWARE DETAILS

4.1 ABOUT DE1 BOARD

The purpose of this board is to provide the ideal vehicle for learning about digital logic, computer organization, and FPGAs. It uses the state-of-the-art technology in both hardware and CAD tools to expose students and professionals to a wide range of topics. The board offers a rich set of features that make it suitable for use in alaboratory environment for university and college courses, for a variety of design projects, as well as for the development of sophisticated digital systems. Altera provides a suite of supporting materials for the DE1 board, including tutorials, “ready-to-teach” laboratory exercises, and illustrative demonstrations.

4.2 SUPPORTING MATERIAL

Software provided with the DE1 board features the Quartus® II Web Edition CAD system, and the Nios® II Embedded Processor. Also included are

several aids to help students and professionals experiment with features of the board, such as tutorials and example applications.

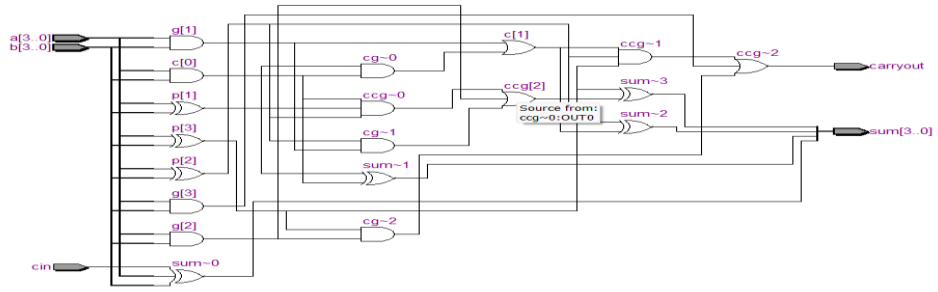
Traditionally, manufacturers of educational FPGA boards have provided a variety of hardware features and software CAD tools needed to implement designs on these boards, but very little material has been offered that could be used directly for teaching purposes. Altera's DE1 board is a significant departure from this trend. In addition to the DE1 board's hardware and software, Altera Corporation provides a full set of associated *laboratory exercises* that can be performed in a laboratory setting for typical courses on logic design and computer organization. In effect, the DE1 board and the available exercises can be used as a readyto-teach platform for both university and college courses.

4.3 ENGINEERING PROFESSIONALS

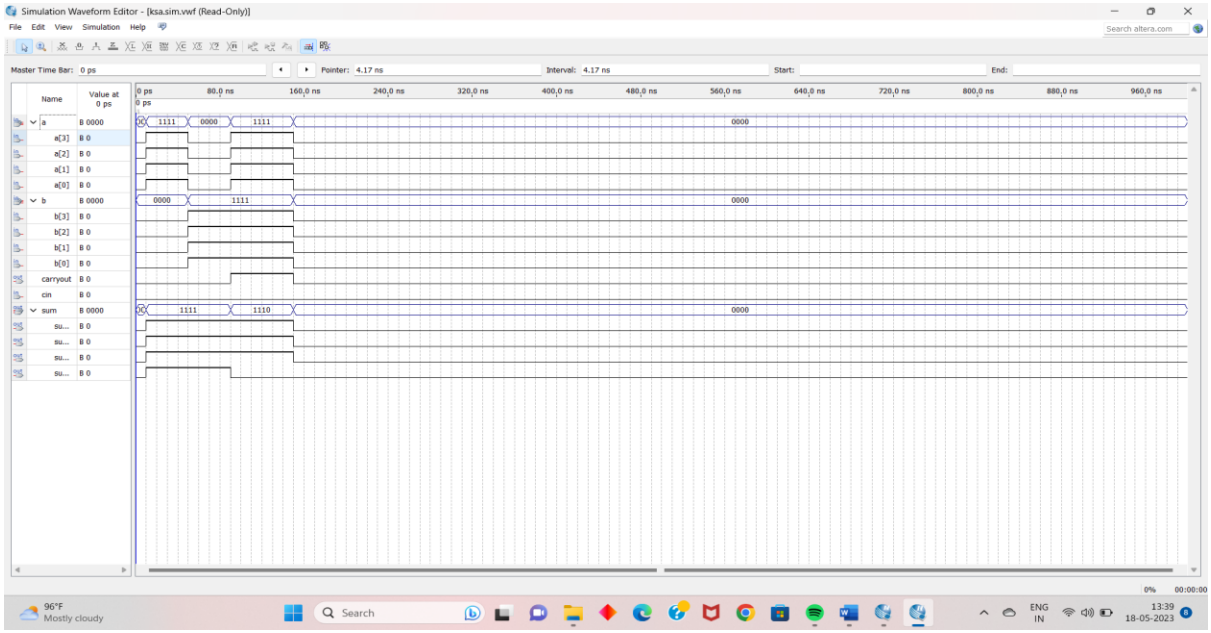
With its advanced Cyclone® II FPGA, flexible memory options, and a plethora of advanced I/O devices, the DE1 board is an ideal platform for the implementation of many types of digital systems. Engineering professionals will appreciate the wealth of design examples provided with the board, and will enjoy experimenting with audio, video. The DE1 board is an ideal vehicle for implementing embedded applications such as those that feature the Altera Nios II embedded processor.

5.RESULTS

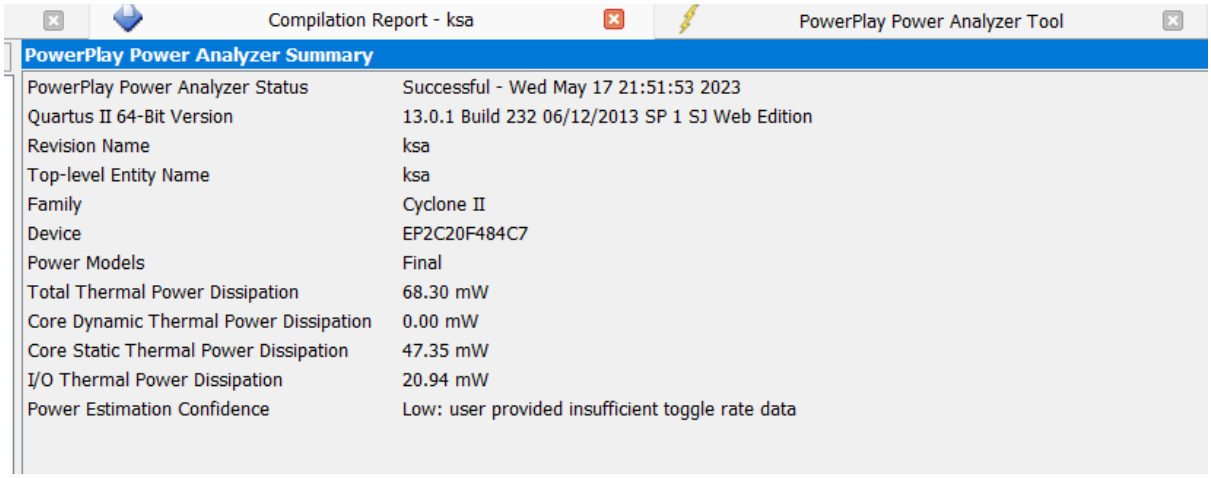
5.1. KOGGE STONE ADDER



RTL VIEWER



WAVEFORM



POWER SUMMARY REPORT

Compilation Report - ksa

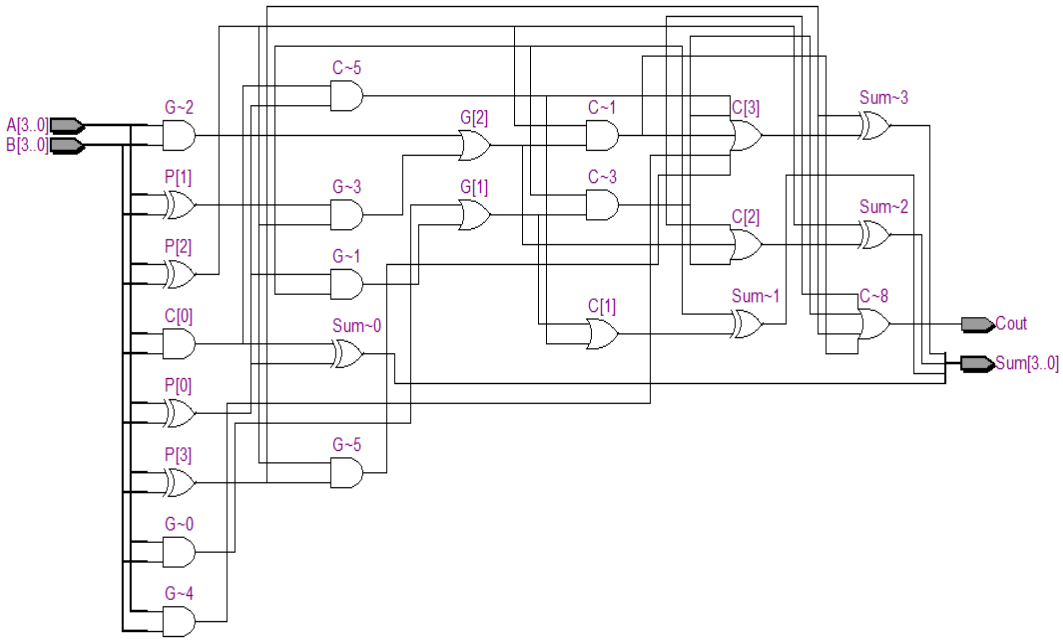
Progagation Delay

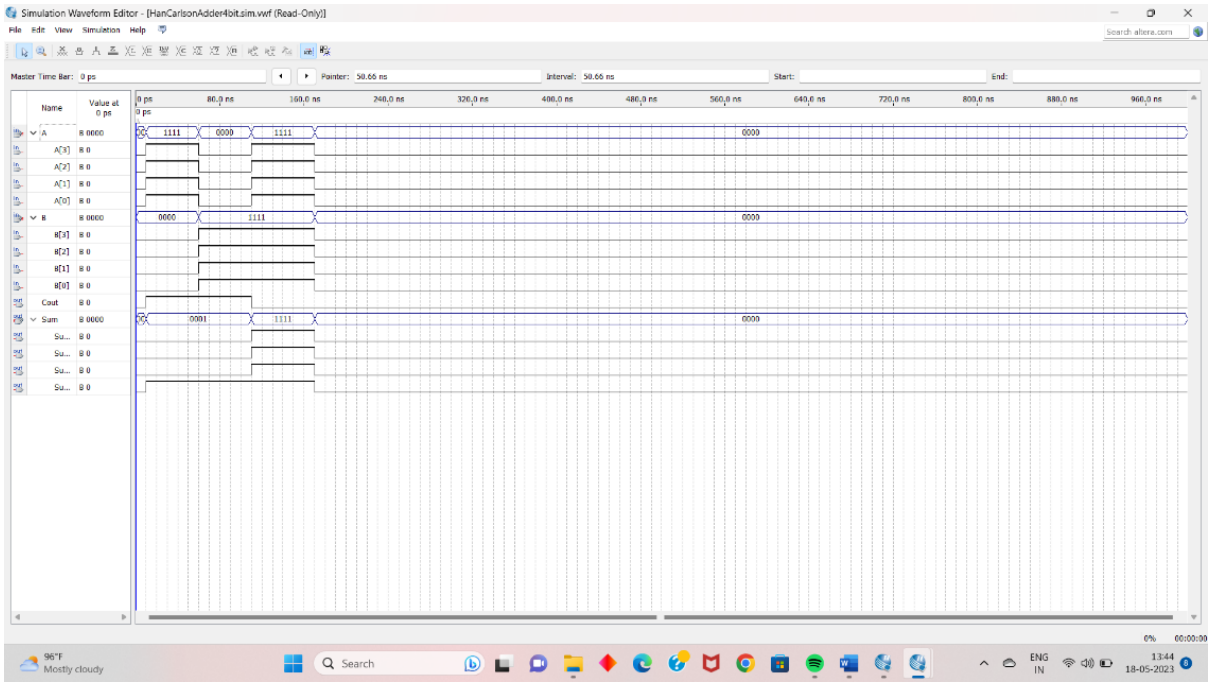
	Input Port	Output Port	RR	RF	FR	FF
1	a[0]	carryout	12.499			12.499
2	a[0]	sum[0]	11.732	11.732	11.732	11.732
3	a[0]	sum[1]	11.997	11.997	11.997	11.997
4	a[0]	sum[2]	12.745	12.745	12.745	12.745
5	a[0]	sum[3]	11.923	11.923	11.923	11.923
6	a[1]	carryout	12.434			12.434
7	a[1]	sum[1]	11.927	11.927	11.927	11.927
8	a[1]	sum[2]	12.680	12.680	12.680	12.680
9	a[1]	sum[3]	11.862	11.862	11.862	11.862
10	a[2]	carryout	11.232			11.232

PROPAGATION DELAY REPORT

5.2 HAN-CARLSON ADDER

RTL VIEWER





WAVEFORM

POWER SUMMARY REPORT

Compilation Report - HanCarlsonAdder4bit

PowerPlay Power Analyzer Tool

PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Wed May 17 20:26:02 2023
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	HanCarlsonAdder4bit
Top-level Entity Name	HanCarlsonAdder4bit
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	68.22 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	20.87 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

PROPAGATON DELAY REPORT

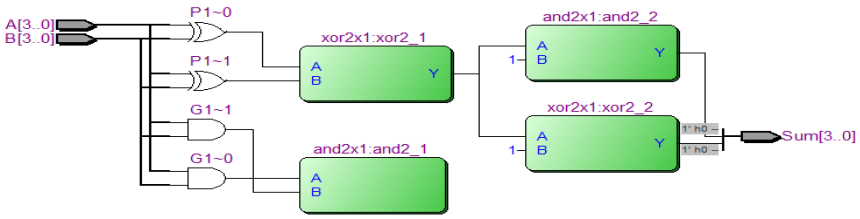
Compilation Report - HanCarlsonAdder4bit

Propagation Delay

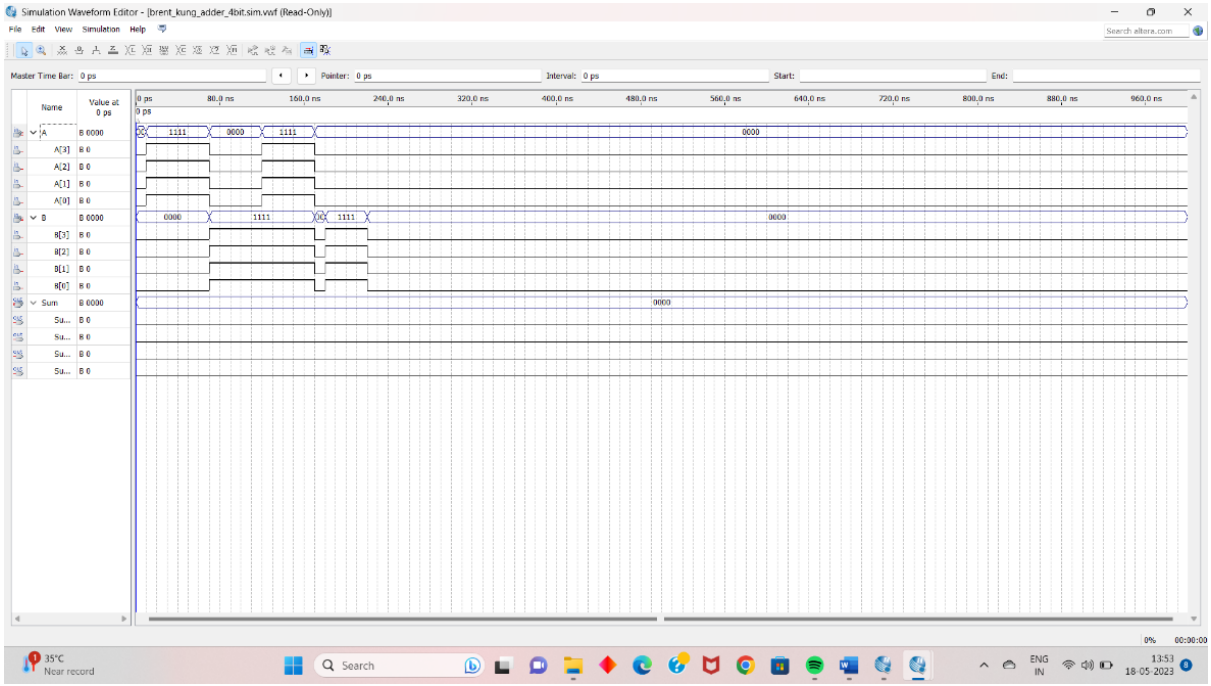
	Input Port	Output Port	RR	RF	FR	FF
1	A[0]	Cout	5.753	5.753	5.753	5.753
2	A[0]	Sum[0]	5.478			5.478
3	A[0]	Sum[1]	5.592	5.592	5.592	5.592
4	A[0]	Sum[2]	5.913	5.913	5.913	5.913
5	A[0]	Sum[3]	5.928	5.928	5.928	5.928
6	A[1]	Cout	5.641	5.641	5.641	5.641
7	A[1]	Sum[1]	5.480			5.480
8	A[1]	Sum[2]	5.801	5.801	5.801	5.801
9	A[1]	Sum[3]	5.816	5.816	5.816	5.816
10	A[2]	Cout	6.367	6.367	6.367	6.367

6.3 BRENT-KUNG ADDER

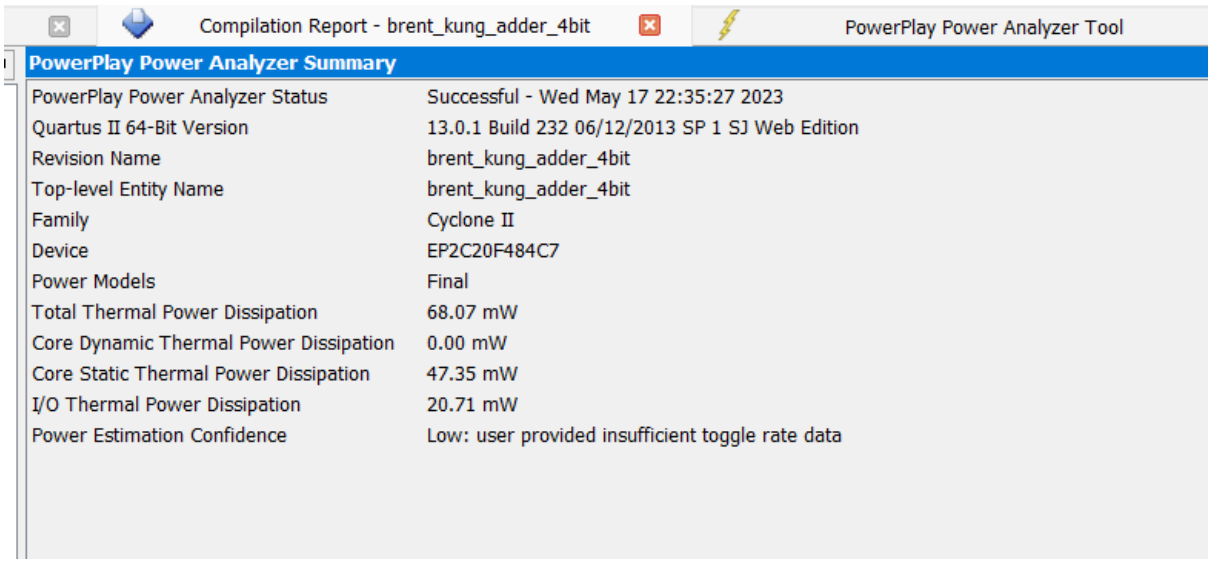
RTL VIEWER



WAVEFORM



POWER SUMMARY REPORT

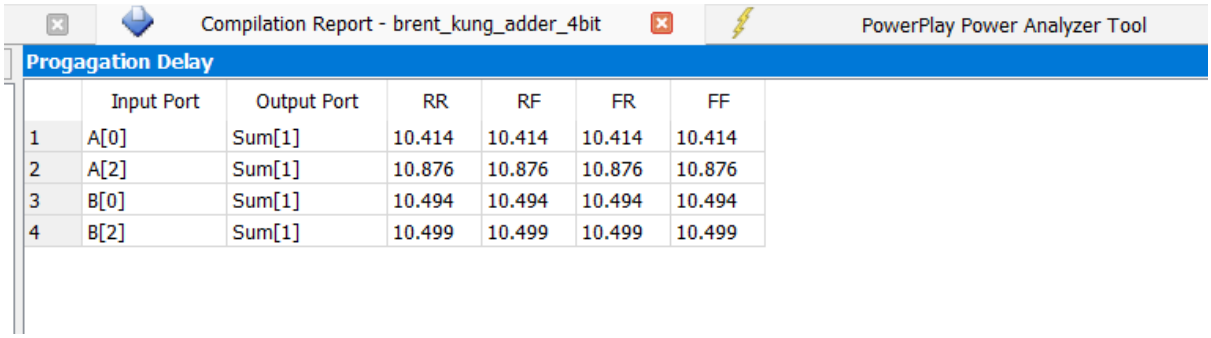


Compilation Report - brent_kung_adder_4bit | PowerPlay Power Analyzer Tool

PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Wed May 17 22:35:27 2023
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	brent_kung_adder_4bit
Top-level Entity Name	brent_kung_adder_4bit
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	68.07 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	20.71 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

PROPAGATION DELAY REPORT



Compilation Report - brent_kung_adder_4bit | PowerPlay Power Analyzer Tool

Progagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	A[0]	Sum[1]	10.414	10.414	10.414	10.414
2	A[2]	Sum[1]	10.876	10.876	10.876	10.876
3	B[0]	Sum[1]	10.494	10.494	10.494	10.494
4	B[2]	Sum[1]	10.499	10.499	10.499	10.499

6.CONCLUSION

In summary, Kogge-Stone, Brent-Kung, and Han-Carlson are three Parallel Prefix adder architectures that excel in different aspects while efficiently performing addition operations. The Kogge-Stone architecture is known for its high speed and scalability. It achieves this by employing a large number of Parallel carry computations, allowing for efficient propagation of carry signals. However, a drawback of Kogge-Stone is its increased area complexity due to the extensive interconnections required. On the other hand, the Brent-Kung architecture strikes a balance between speed and area complexity. It reduces the number of interconnections compared to Kogge-Stone, resulting in a more compact design and improved circuit complexity. Brent-Kung adders are often

favored for applications that require a reasonable compromise between performance and circuit complexity. Han-Carlson adders combine the strengths of both Kogge-Stone and Brent-Kung architectures. They leverage a hierarchical structure to achieve a balance between performance and area complexity while also providing a high level of scalability. Han-Carlson adders are particularly advantageous for applications that require both speed and efficient use of circuit area. Ultimately, the choice of the Parallel Prefix adder architecture depends on the specific requirements of the application. Factors such as desired speed, area utilization, and scalability play a crucial role in determining which architecture is the most suitable. By considering these factors, designers can make an informed decision to optimize the performance of their adder implementation.

DELAY PERFORMANCE ANALYSIS OF VARIOUS PARALLEL PREFIX ADDERS:

Adders	Propagation Delay
Kogge Stone adder	12.499
Brent-Kung adder	10.414
Han-carlson adder	5.753

POWER ANALYSIS OF VARIOUS PARALLEL PREFIX ADDERS:

Adders	Total thermal power dissipation(mw)	Core Dynamic Thermal power dissipation(mw)	Core Static Thermal power dissipation(mw) (mw)	I/O Thermal Power dissipation(mw)
Kogge Stone adder	68.30	0.00	47.35	20.71
Brent-kung adder	68.07	0.00	47.35	20.71
Han-carlson adder	68.22	0.00	47.35	20.87

AN EFFICIENT AND LOW POWER FULL ADDER CIRCUIT USING XOR XNOR GATES

DINESHWARAN S, JUSTUS RAJA J

ABSTRACT

Here, innovative circuits for XOR/XNOR and simultaneous XOR– XNOR functions are proposed. The proposed circuits are highly optimized in terms of the power consumption and delay, which are due to low output capacitance and low short-circuit power dissipation. We also proposed hybrid 1-bit full-adder (FA) circuits based on the novel full-swing XOR/XNOR gates. Each of the proposed circuits has its own merits in terms of speed, power consumption, power- delay product (PDP), driving ability, and so on.

To investigate the performance of the proposed designs, extensive Mentor Graphics simulations are performed. The simulation results, based on the 65-nm CMOS process technology model, indicate that the proposed designs have superior speed and power against other FA designs. A new transistor sizing method is presented to optimize the PDP of the circuits. In the proposed method, the numerical computation particle swarm optimization algorithm is used to achieve the desired value for optimum PDP with fewer iterations. The proposed circuits are investigated in terms of variations of the supply and threshold voltages, output capacitance, input noise immunity, and the size of transistors.

1 INTRODUCTION

Nowadays, electronic systems are an inseparable part of everyday life. Digital circuits, like microprocessors, digital communication devices, and digital signal processors, comprise a large part of electronic systems. As the scale of integration increases, the usability of circuits is restricted by the augmenting amounts of power and area consumption. Therefore, with the growing popularity and demand for the battery-operated portable devices such as mobile phones,

tablets, and laptops, the designers try to reduce power consumption and area of such systems while preserving their speed.

Optimizing the W/L ratio of transistors is one approach to decrease the power delay product(PDP) of the circuit while preventing the problems resulted from reducing the supply voltage. The efficiency of many digital applications relates to the performance of the arithmetic circuits, such as adders, multipliers, and dividers. Due to the fundamental role of addition in all the arithmetic operations, many efforts have been made to explore efficient adder structures, e.g., carry select adders, carry skip adders, conditional sum adders, and carry look ahead adders. Full adder (FA) as the fundamental block of these structures is at the center of attention.

1.1 MENTOR GRAPHICS

Mentor Graphics was a company that provided electronic design automation (EDA) software and services. However, as of the knowledge cutoff in September 2021, Mentor Graphics was acquired by Siemens PLM Software and is now part of the Siemens Digital Industries Software division. The EDA tools and software formerly offered by Mentor Graphics are now integrated into Siemens' portfolio. Mentor Graphics (now Siemens) offers a wide range of software solutions for various aspects of electronic design, including:

Integrated Circuit (IC) Design: Mentor Graphics provides tools for designing and verifying complex integrated circuits, such as digital, analog, and mixed-signal designs. These tools help engineers with tasks like schematic capture, simulation, physical layout, and verification. Automotive Electronics: Mentor Graphics provides software solutions specifically tailored for designing automotive electronic systems, including electrical and wire harness design, simulation, and verification.Embedded Systems: The company offers tools for developing and testing embedded software for various applications, including automotive, aerospace, and consumer electronics.

Functional Safety: Mentor Graphics provides software solutions to help engineers achieve functional safety standards, such as ISO 26262 for automotive systems.

1.2 TANNER S-EDIT TOOL

Tanner S-Edit is an easy-to-use design environment for schematic capture and design entry. It gives you the power you need to handle your most complex mixed-signal IC design capture. S-Edit is tightly integrated with Tanner T-Spice, Analog FastSPICE (AFS), or Eldo simulators, the Tanner L-Edit IC layout tool, and the Calibre LVS and PEX tools.

S-Edit helps you meet the demands of today's fast-paced market by optimizing your productivity and speeding your concepts to silicon. A faster design cycle gives you more flexibility in moving to an optimal solution, freeing up more time and resources for process corner validation. The results are less risk downstream, higher yield, and quicker time to market.It increases your design productivity while handling the most complex IC designs. This powerful environment supports fast, 64- bit rendering and cross-probing between schematic, layout, simulator and LVS reporting at net and device levels.

Instances in the schematic are linked to simulation models for the designers choice of behavioural modelling from transistor level SPICE to HDL blocks (Verilog or VHDL). Out of the box, S-Edit is integrated with several analog transistor level simulators and mixed signal simulation platforms to suit the users needs. These include AFS, Eldo and T-Spice simulators for SPICE simulation and Questa ADMS and Symphony for co-simulation with digital portions of a design.It works with version control platforms. All but the simplest of IC design teams should consider applying version control to their design infrastructure. Even single person designs benefit from ability to track file versions and employ file set configurations. Growing to multi-engineer /multisite collaboration and design data management is critical. Tanner S-Edit integrates with solutions from ClioSoft and Perforce.

1.3 OBJECTIVE

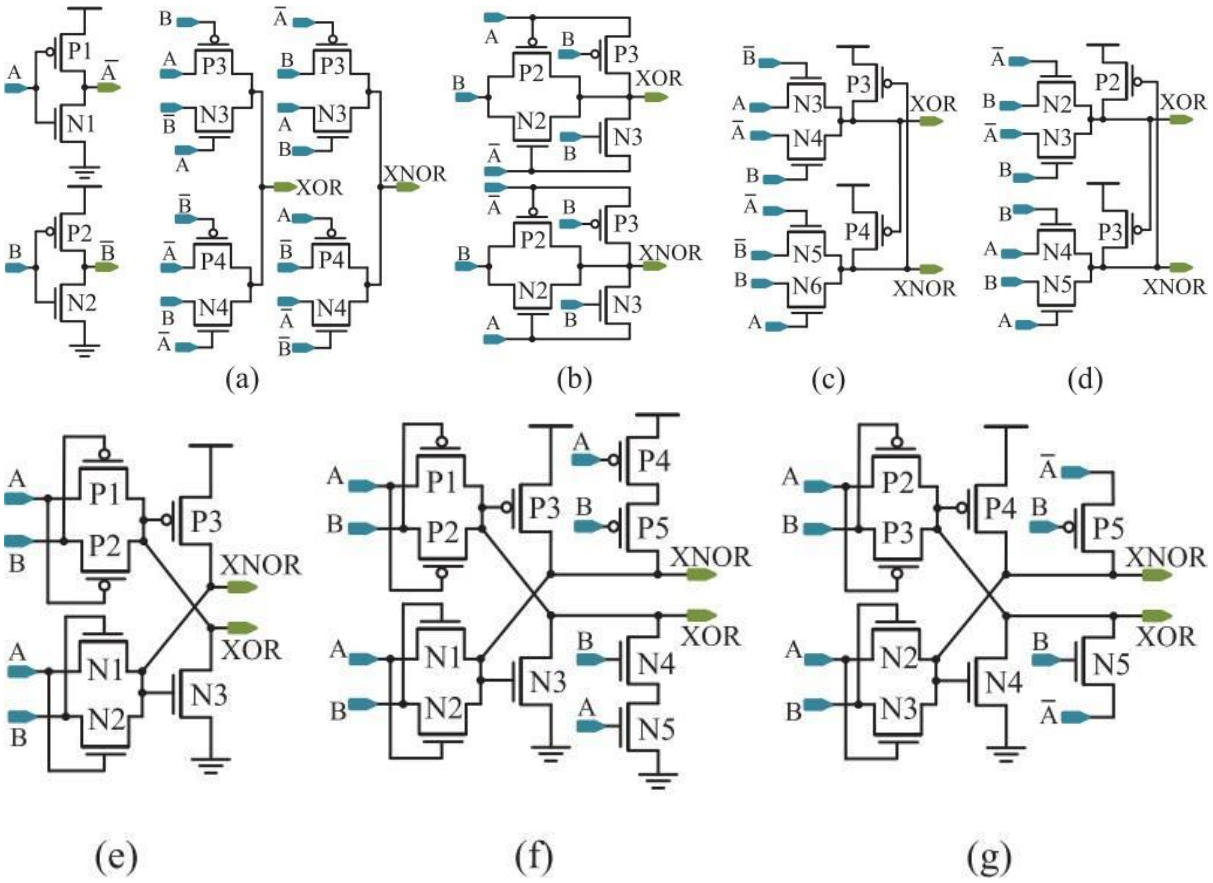
In this Project, the main focus is on designing and evaluating various Full Adders to determine their efficiency based on different parameters. The motivation behind this investigation is to overcome the time delay and power issues associated with traditional adders, which have low output capacitance and low short circuit power dissipation resulting in slower operation times and higher power consumption. Also, we try to remove the problems present in the investigated circuits. Afterwards, with these new XOR/XNOR circuits, we propose six Full Adder structures.

2. CIRCUIT ANALYSIS

2.1 REVIEW OF XOR, XNOR CIRCUITS

XOR or Ex-OR and XNOR gates are special type of gates used in the adders and subtractors. These has n input (n>=2) and one output. To build the adders many logic gates can be used but the XOR/XNOR gates plays a efficient role. To design the adders we proposed XOR/XNOR circuits and simultaneous XOR-XNOR circuits. The XOR/XNOR gate is the major consumer of power in the Adders. Therefore, the power consumption of the Adders cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design.

Hybrid FAs are made of two modules, including 2-input simultaneous XOR/XNOR gate and 2-to-1 multiplexer (2-1-MUX) gate . The XOR/XNOR gate is the major consumer of power in the FA cell. Therefore, the power consumption of the FA cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design. Many circuits have been proposed to implement XOR/XNOR gate [11],[16], [23], which a few examples of the most efficient ones are shown in Fig.3.1



(a) and (b) Full-swing XOR/XNOR and (c)–(g) XOR–XNOR circuits

This structure has eight transistors. The main problem of this circuit is using two high power consumption NOT gates on the critical path of the circuit, because the NOT gates must drive the output capacitance. Therefore, the size of the transistors in the NOT gates should be increased to obtain lower critical path delay. Further more, it causes the creation of an intermediate node with a large capacitance. Of course, this means that the NOT gates drives the output of circuit through, for example, pass transistor or TG. Therefore, the short-circuit power and, thus, the total power dissipation of this circuit are widely increased.

Moreover, in the optimum PDP situation, the critical path delay will also be increased slightly. Fig.3.1(b) shows another example of the full-swing XOR/XNOR gate [11], each made of six transistors. This circuit is based on the PTL logic style, whose delay and power consumption are better than the circuit depicted in Fig.3.1(a). The only problem of this structure is using a NOT gates

on the critical path of the circuit. The XOR circuit of Fig.3.1(b) has the lower delay than its XNOR circuit, because the critical path of XOR circuit is comprised of a NOT gates with an NMOS transistor (N3). But the critical path of XNOR circuit is comprised of a NOT gates and a PMOS transistor (P5) (PMOS transistor is slower than NMOS transistor). Therefore, to improve the XNOR circuit speed, the size of PMOS transistor (P5) and NOT gates should be increased.

2.2 SIMULTANEOUS XOR–XNOR CIRCUITS

In recent years, the simultaneous XOR–XNOR circuit is widely used in hybrid Full Adder structures [3], [9], [16], [18]. Commonly, in the hybrid Full Adders, the XOR–XNOR signals are connected to the inputs of 2-1-MUX as select lines. Therefore, two simultaneous signals with the same delay are necessary to avoid glitches in the output nodes of the FA.

Fig.3.1(c) shows an example of the simultaneous XOR–XNOR circuit [16]. This circuit is based on the CPL logic style that has been designed by using ten transistors. In this structure, the outputs have been driven only by NMOS transistor, and thus, two PMOS transistors are connected to outputs (XOR and XNOR) as cross coupled to recover the output-level voltages. One problem of this XOR–XNOR circuit is to have the feedback (cross-coupled structure) on the outputs, which increases the delay and short-circuit power of this structure. Therefore, to mitigate the imposed delay, the size of transistors should be increased.

Another disadvantage of this structure is the existence of two NOT gates in the critical path. Goel et al. [3] removed two transistors (a NOT gates) from the XOR–XNOR circuit of Fig. 3.1(c) to reduce the power dissipation of the circuit. In Fig. 3.1(d), when the inputs are in AB = 00, the transistors N3, N4, and N5 are turned OFF and logic “0” is passed through the transistor N2 to XOR output. This “0” on XOR charges the XNOR output to VDD by transistor P3. Therefore, the critical path of this circuit is larger than that of the circuit of Fig. 3.1(c). Also, in

this structure, the short-circuit current will be passed through the circuit when the input is changed from AB = 01 to AB = 00. When the inputs are in state AB = 01, logic “1” is passed through the transistors N2, N3, and P2 to XOR output and logic “0” is passed through the transistor N4 to XNOR output.

When the inputs change to AB = 00, all transistors will be turned OFF except transistors N2 (through the input A) and P2 (through the XNOR output, which has not changed now).Therefore, the short-circuit current will pass from the transistors P2 and N2. If the amount of current being sourced from the transistor P2 is larger than that of current being sunk from the transistor N2, the short-circuit current will continue to be drawn from VDD and will never switch XOR and XNOR output. This situation also occurs when the input is changed from AB = 11 to AB = 10 and impacts the proper functioning of the circuit. To grantee the proper operation of this circuit, the ON-state resistance of transistors P2 and P3 should not be smaller than that of transistors N2 and N5 (RP2 > RN2, RP3 > RN5), respectively. Furthermore, this structure is very sensitive to process variation; if the size of transistors is changed, the circuit may not operate properly.

2.3 PROPOSED CIRCUITS

The non full-swing XOR/XNOR circuit of Fig.3.2(a) is efficient in terms of the power and delay. Furthermore, this structure has an output voltage drop problem for only one input logical value. To solve this problem and provide an optimum structure for the XOR/XNOR gate, we propose the circuit shown in Fig.3.2(b). For all possible input combinations, the output of this structure is full swing. The proposed XOR/XNOR gate does not have NOT gates on the critical path of the circuit. Thus, it will have the lower delay and good driving capability in comparison with the structures of Fig.3.1(a) and (b). Although the proposed XOR/XNOR gate has one more transistor than the structure of Fig.3.1(b), it demonstrates lower power dissipation and higher speed.

DESIGNS	N1 P1 N2 P2 N3 P3 N4 P4 N5 P5 N6 P6	DELAY	POWER	PDP
Fig.3.1(a) XOR	130 610 180 130 130 130 130 262	26..1	2.48	64.7
XNOR	195 130 130 640 130 130 155 240	25.8	2.50	64.5
Fig. 3.1(b) XOR	342 130 130 190 166 250	23.6	2.14	505
XNOR	130 793 130 130 130 456	25.6	2.47	63.2
Fig. 3.1(b) XOR	130 130 330 245 170 344 130	21.9	2.22	48.6
XNOR	130 130 204 732 130 578 130	21.5	2.46	52.9

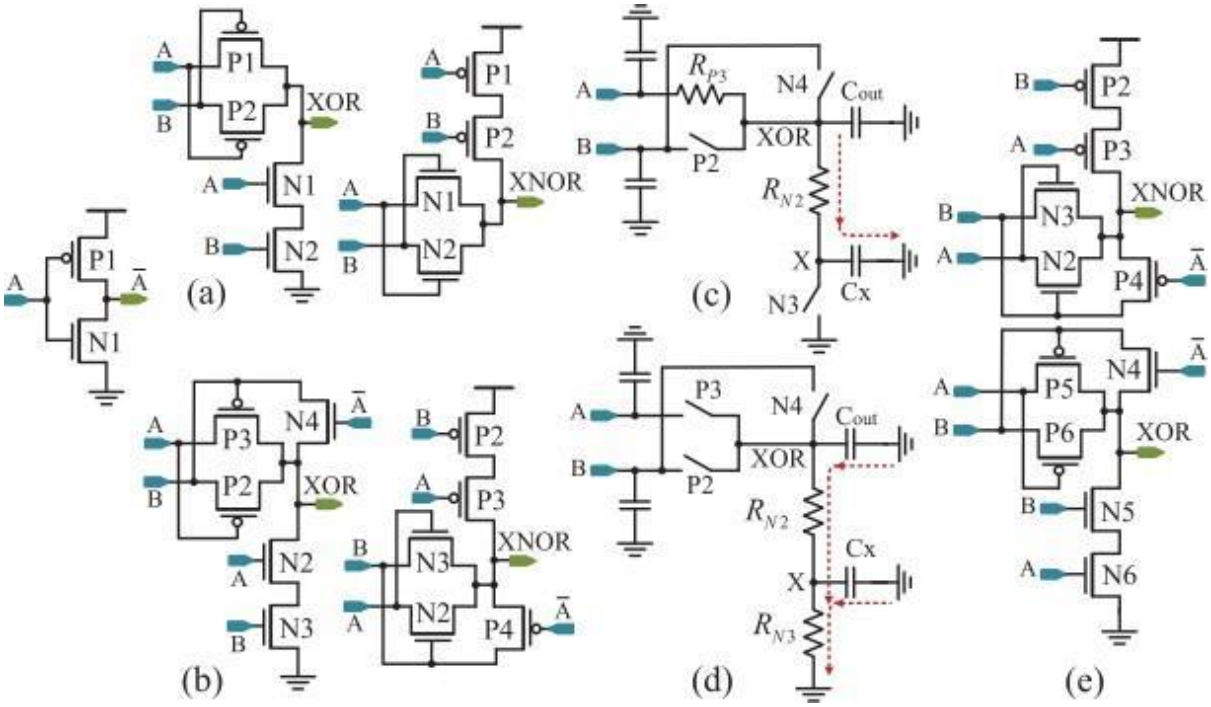
Simulation results (optimum size of transistors in nm, power in e- 6w, delay in ps, and pdp in aj) for xor/xnor crcuits in 65-nm tech with 1.2-v power supply voltage at 1 ghz

2.4 PROPOSED XOR–XNOR CIRCUIT

Fig. shows the proposed structure of the simultaneous XOR–XNOR gate consisting of 12 transistors. This structure is obtained by combining the two proposed XOR and XNOR circuits of Fig.3.2(b). If the inputs of this circuit are connected as mentioned in Section III-A, the input A and B capacitances are not equal (the inputs A and B are connected to the same transistor count). Thus, to equal the input of capacitances, they are connected to the circuit, as shown in Fig.3.2(e). In this case, the input capacitances are approximately equal and the power and delay are optimized. This structure does not have any NOT gates on the critical path and its output capacitance is very small. For this reason, it is very

high speed and consumes low power. The delay of XOR and XNOR outputs of this circuit is almost identical, which reduces the glitch in the next stage. Other advantages of this circuit are good driving capability, full-swing output, as well as robustness against transistor sizing and supply voltagescaling.

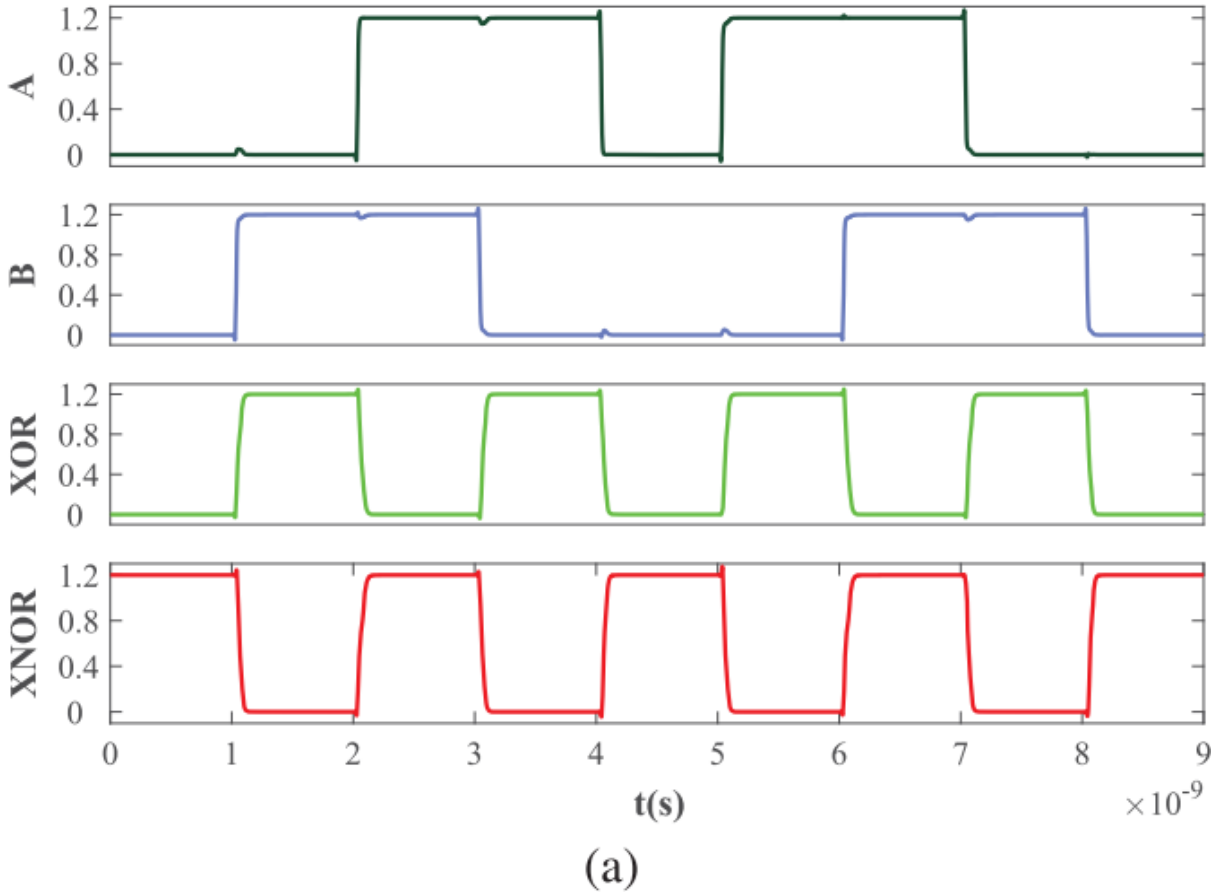
The proposed XOR/XNOR and simultaneous XOR–XNOR structures were compared with all the above-mentioned structures (Fig.3.1). The simulation results at TSMC 65-nm technology and 1.2-V power supply voltage (VDD) are shown in Table 3.1. The input pattern is used as all possible input combinations have been included [Fig.3.3(a)]. The maximum frequency for the inputs was 1 GHz and 4× unit-size inverter was connected to the output (as a load). The size of transistors has been selected for optimum PDP by using the proposed transistor sizing method, which the proposed procedure will be described earlier.



(a) Non full-swing XOR/XNOR gate. (b) Proposed full-swing XOR/XNOR gate. (c) RC model of proposed XOR for AB = 10. (d) RC model of proposed XOR for AB = 11. (e) Proposed XOR–XNOR gate

The optimum size of transistors for each XOR/XNOR and XOR–XNOR circuits are expressed in Table 3.1. In the output rise and fall transition, the delay is calculated from 50% of the input voltage level to 50% of the output voltage level.

The PDP will be calculated by multiplying the worst case delay by the average power consumption of the main circuit.



(a)

Simulation results of XOR–XNOR circuits.

The results indicate that the performance of the proposed XOR/XNOR and simultaneous XOR–XNOR structures is better than that of the compared structures. The proposed XOR and XNOR circuits [Fig.3.2(b)] have the lowest PDP and delay, respectively, compared with other XOR/XNOR circuits. Also, the delay of these two proposed circuits is very close together that prevents the creation of glitch on the next stage. The delay, power consumption, and PDP of the XOR and XNOR circuits of Fig.3.1(a) are almost equal, due to having the same structures. As mentioned earlier and according to the obtained results, the XOR circuit of Fig.3.1(b) has a better performance than its XNOR circuit. The proposed circuit for simultaneous XOR–XNOR has better efficiency in all three

calculated parameters (delay, power dissipation, and PDP) when it is compared with other XOR–XNOR gates. The proposed XOR-XNOR circuit is saving almost 16.2%-85.8% in PDP ,and it is 9%-83.2% faster than the other circuits. The circuits of Fig.3.1(d) and (e) have the very high delay due to its output feedback (which have the slow response problem).

$$PDP_n = \frac{T_{d_{AB=10\to11}} \times P_{AB=10\to11}}{CR_{\min} \times CV_{DD}{}^2} = \left[3\left(\frac{1}{k_{N2}}+\frac{1}{k_{N3}}\right)+2\left(1+\frac{k_{N2}}{k_{N3}}\right)\right](2k_{N2}+2k_{N3}+6).$$

As can be seen in Table 3.1, the efficiency of Fig.3.1(e) is much worse and its delay is four times more than that of other circuits.

Table 3.1 indicates that the structures have shown a better performance, which have the minimum NOT gates on the critical path and also have not feedback on the outputs to correct the output voltage level.

2,5 PROPOSED FULL ADDER

We proposed six new Full Adder circuits for various applications which have been shown in Fig.3.4 Also, Fig. 3.5 shows the circuit layout of proposed Full Adder cell shown in Fig. 3.4(a). These new Full Adders have been employed switch hybrid logic style, and all of them are designed by using the proposed XOR/XNOR circuit. The well-known four-transistor 2-1-MUX structure is used to implement the proposed hybrid Full Adder cells. A 2-1- MUX is created with TG logic style that has no static and short-circuit power dissipation. Fig. 3.4(a) shows the circuit of first proposed hybrid Full Adder (HFA-20T) which is made by two 2-to-1 MUX gates and the XOR–XNOR gate of Fig. 3.2(e).

The circuit of HFA-20T has not high power consumption NOT gates on critical path and consists of 20 transistors. The advantages of this structure are full-swing

output, low power dissipation and very high speed, robustness against supply voltage scaling, and transistor sizing. If A XOR B = 1, then the output C out signal equals to the input signal A or B.

But to equalize the inputs capacitance, both of the input signals A and B are used for implementation and are connected to the transistors N9 and P10 [in Fig. 3.4(a)], respectively. The only problem of HFA-20T is reduction of the output driving capability when it is used in the chain structure applications, such as ripple carry adder. Of course, this problem exists in the circuits that use the transmission function theory in their implementation without buffering output. Fig. 3.5 shows the circuit layout of proposed HFA- 20T which designed for minimum power consumption.

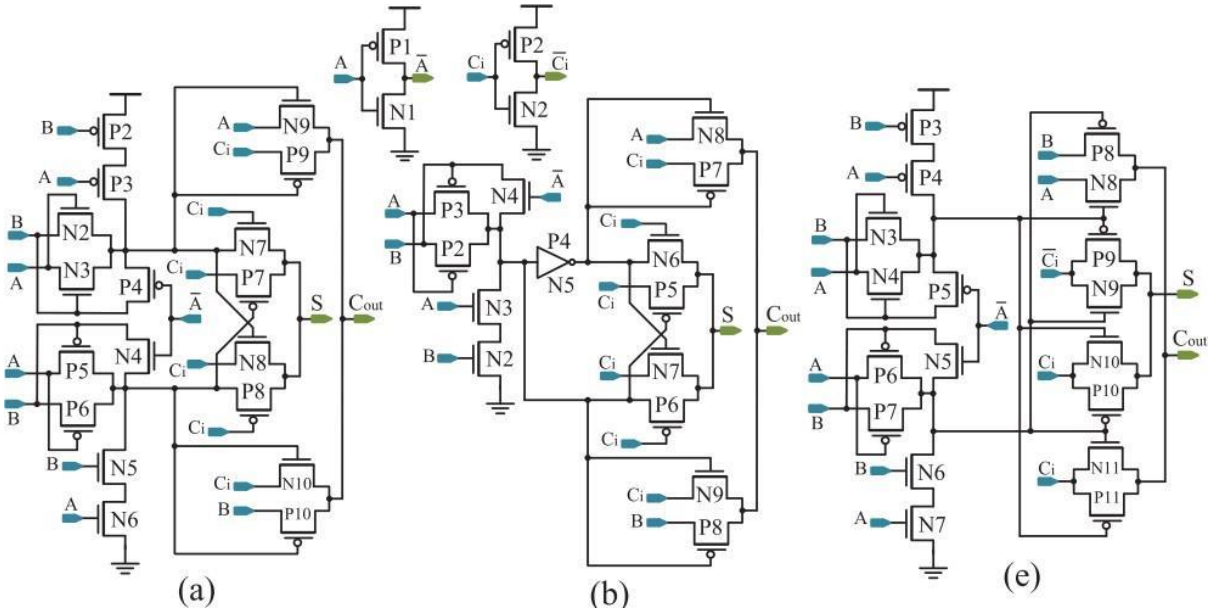
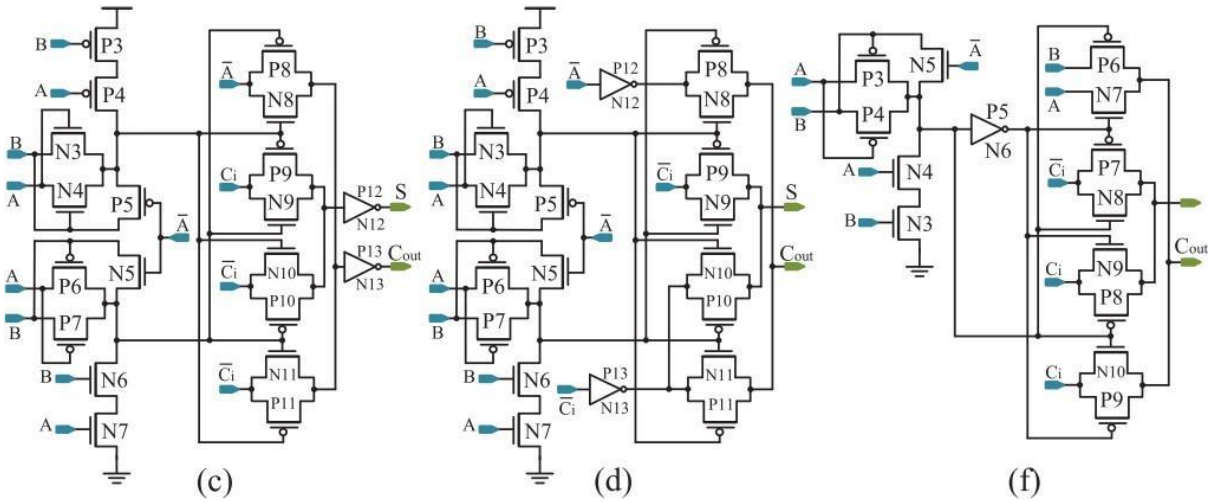


Fig.3.4 (a) HFA-20T. (b) HFA-17T. (c) HFA-B-26T. (d) HFA-NB-26T. (e) HFA-22T. (f) HFA-19T.

The proposed full adders performance is analysed by varying VDD from 0.65 to 1.5v. The results of the simulation for proposed full adders by varying the supply voltage were up to the level. All the proposed full adders work well even for small supply voltage of 0.65v.



Also, by varying the output load from fan out 4 to fan out 64 (FO4 to FO64), the proposed full adders performance is analysed. The supply voltage of 1.2v is used for simulations. The simulation results of proposed full adders by varying the output load are shown in fig.3.5. For the output load of FO64, HFANB-26T has the highest PDP.

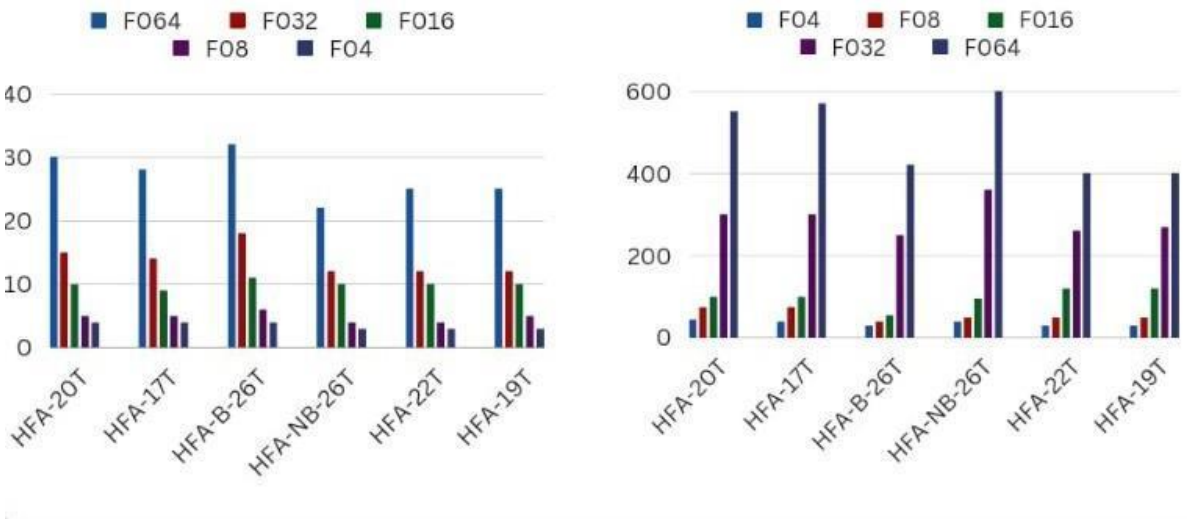


Fig.3.5 Simulation results of proposed full adders with output load variation(a) power consumption (b) delay

3.1 APPLICATIONS

Digital Signal Processing (DSP): DSP algorithms often involve arithmetic operations like addition and multiplication. By incorporating lowpower and fast adders, the performance and energy efficiency of DSP systems can be improved. This is especially valuable in applications such as audio and video processing, image recognition, and wireless communication.Cryptography: Cryptographic algorithms, such as encryption and decryption, heavily rely on arithmetic operations. Low-power and fast adders can enhance the efficiency of cryptographic systems, ensuring secure and energy-efficient data protection in applications like secure communication channels, data storage, and authentication protocols.

Error Correction Codes: Error correction codes, such as ReedSolomon codes, are used to detect and correct errors in data transmission or storage. Low-power and fast adders can accelerate error correction processes, improving the overall efficiency of error detection and correction systems, which are critical in applications like wireless communication, data storage systems, and satellite communications. Image and Video Processing: Image and video processing applications require fast arithmetic operations for tasks like filtering, compression, and transformation. By using low-power and fast adders, the computational speed and energy efficiency of these operations can be enhanced, enabling real-time processing and reducing power consumption in devices such as digital cameras, video recorders, and video streaming platforms.

HPC systems require efficient arithmetic operations for large-scale simulations, scientific computing, and data analysis. Low-power and fast adders can enhance the performance and energy efficiency of HPC architectures, contributing to faster computations, reduced power consumption, and improved scalability.FPGA and ASIC Designs: Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) employ parallel prefix

adders due to their high-speed and area- efficient characteristics. They are used in various digital designs, including communication systems, network routers, and embedded systems.

3.2 ADVANTAGES

Low-power and fast adders using new XOR and XNOR gates offer several advantages compared to traditional adder designs. Here are some key advantages

1. Reduced Power Consumption: Low-power adders are designed to minimize energy consumption during arithmetic operations. By utilizing new XOR and XNOR gates, which are specifically optimized for low power, these adders can significantly reduce power consumption compared to conventional adders. This advantage is particularly important in applications where energy efficiency is critical, such as mobile devices and IoT systems.
2. Improved Speed: Fast adders using new XOR and XNOR gates are designed to enhance the speed of arithmetic operations. These gates are optimized for high-speed operations, resulting in reduced propagation delays and faster computation times. As a result, tasks that involve addition or summation operations can be completed more quickly, leading to improved overall system performance.
3. Area Efficiency: The use of new XOR and XNOR gates can contribute to improved area efficiency in adder designs. These gates can be implemented using compact circuitry, allowing for smaller chip area requirements. This advantage is particularly valuable in applications with space constraints, such as mobile devices and embedded systems.
4. Enhanced Scalability: The new XOR and XNOR gates used in these adder designs often exhibit good scalability properties. This means that as the size of the operands or the complexity of the arithmetic operations increases, the performance and efficiency of these adders can be maintained or even improved.

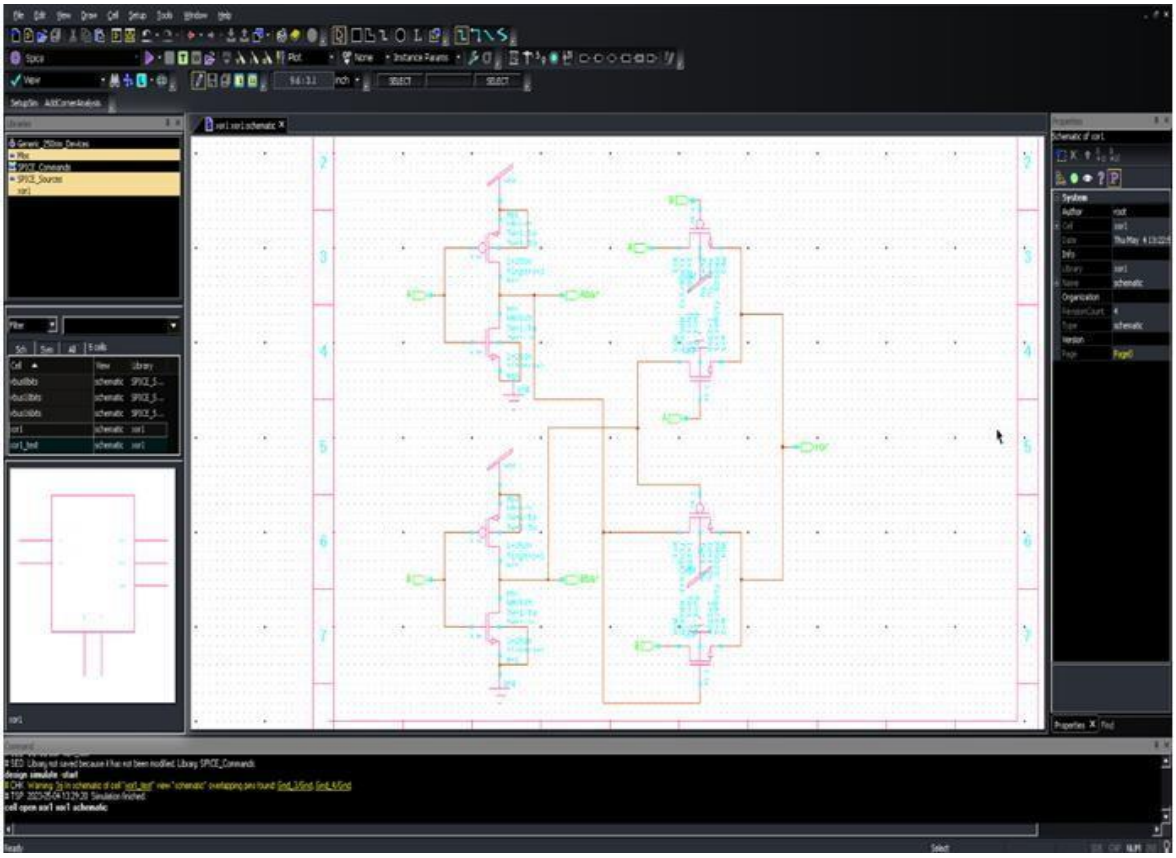
This scalability is crucial in applications that require large-scale computations, such as high-performance computing and data centers.

5. Compatibility with Emerging Technologies: Low-power and fast adders using new XOR and XNOR gates can be designed to be compatible with emerging technologies, such as nanoscale and quantum computing. These adders can be optimized for the characteristics of these technologies, enabling efficient and reliable arithmetic operations in advanced computing systems.

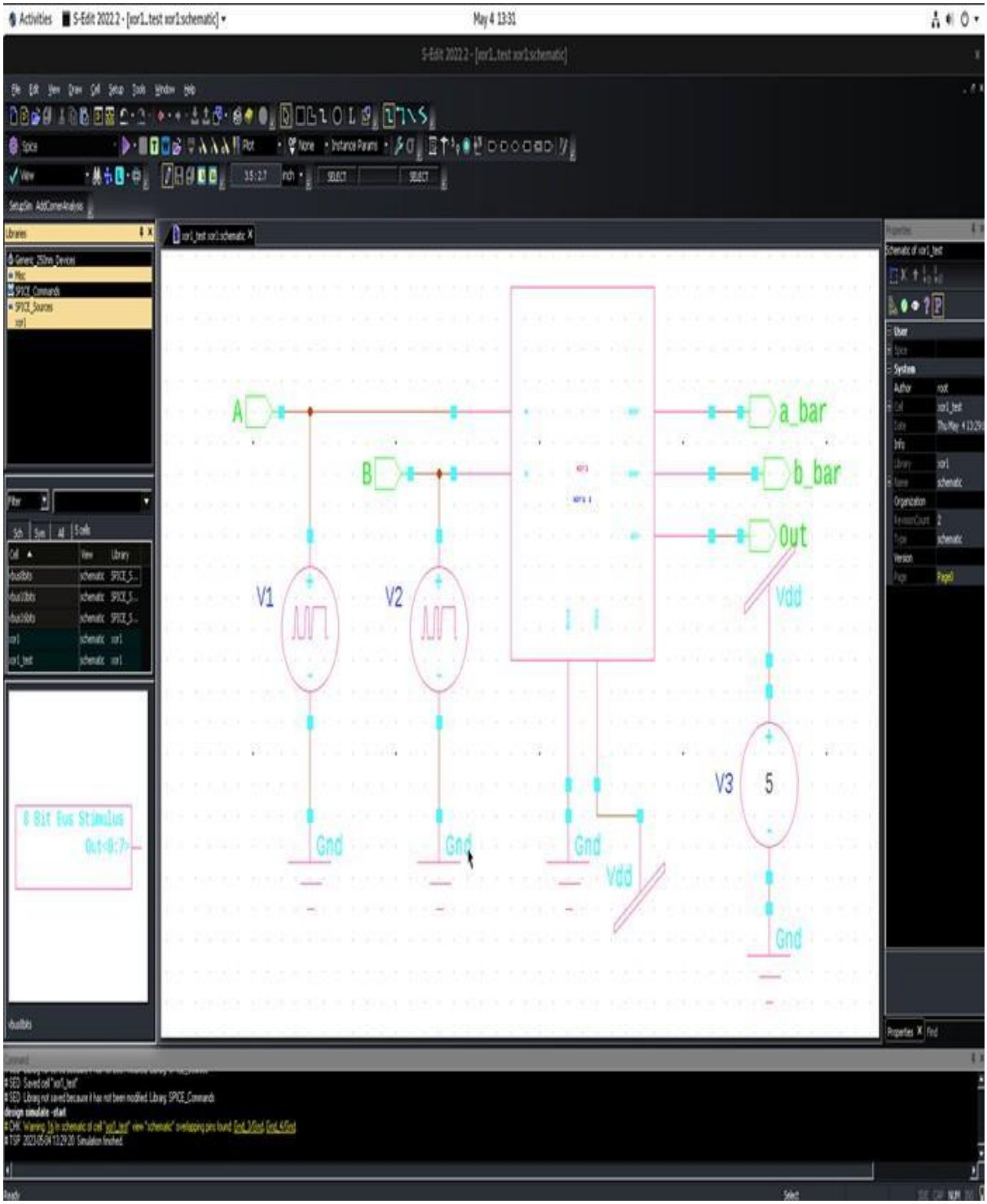
Overall, the advantages of low-power and fast adders using new XOR and XNOR gates include reduced power consumption, improved speed, area efficiency, scalability, and compatibility with emerging technologies. These advantages make them promising candidates for a wide range of applications where efficient and high-performance arithmetic operations are required.

4. RESULTS

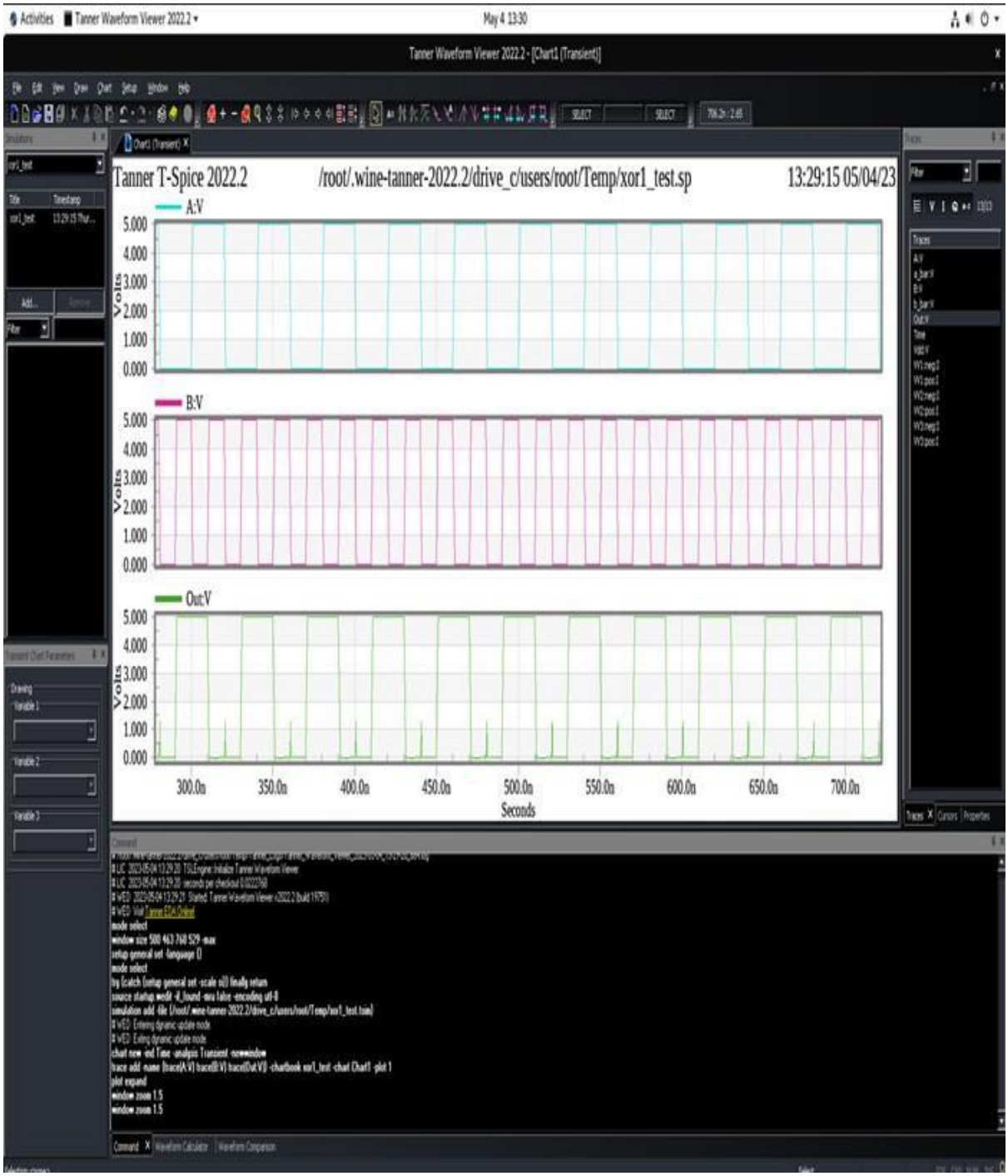
4.1. XOR CIRCUIT



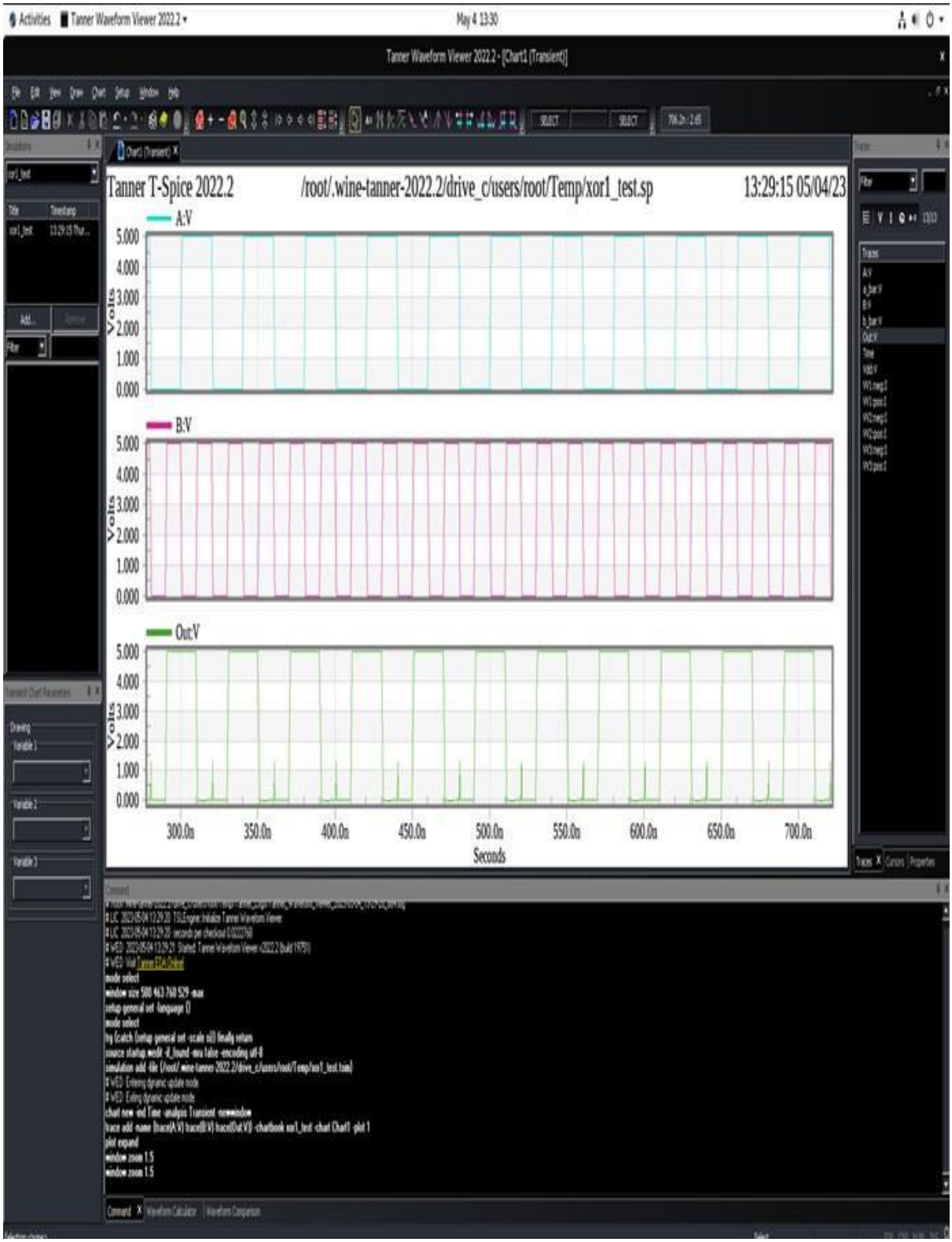
4.2. XOR IC



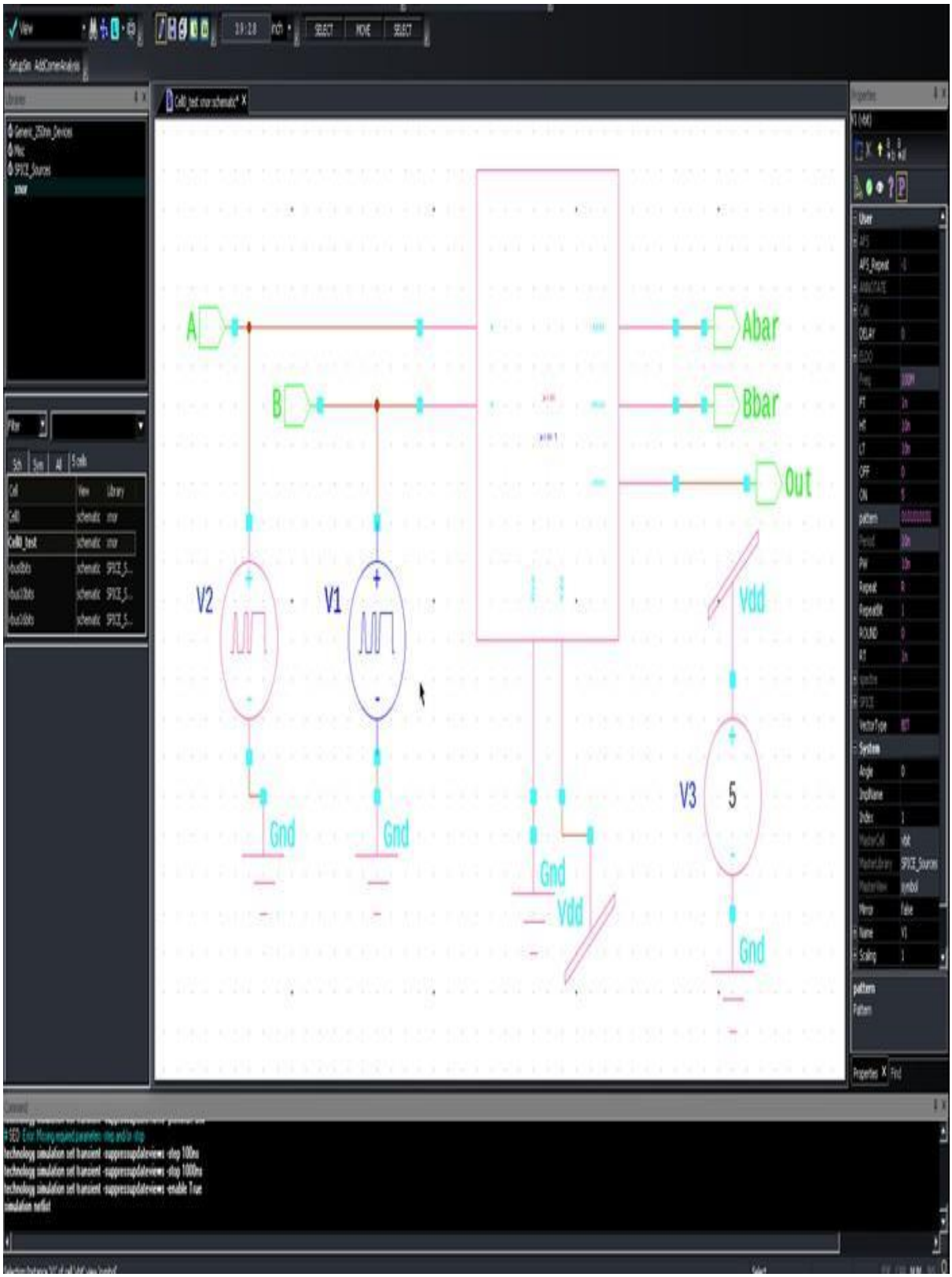
4.3 XOR WAVEFORM



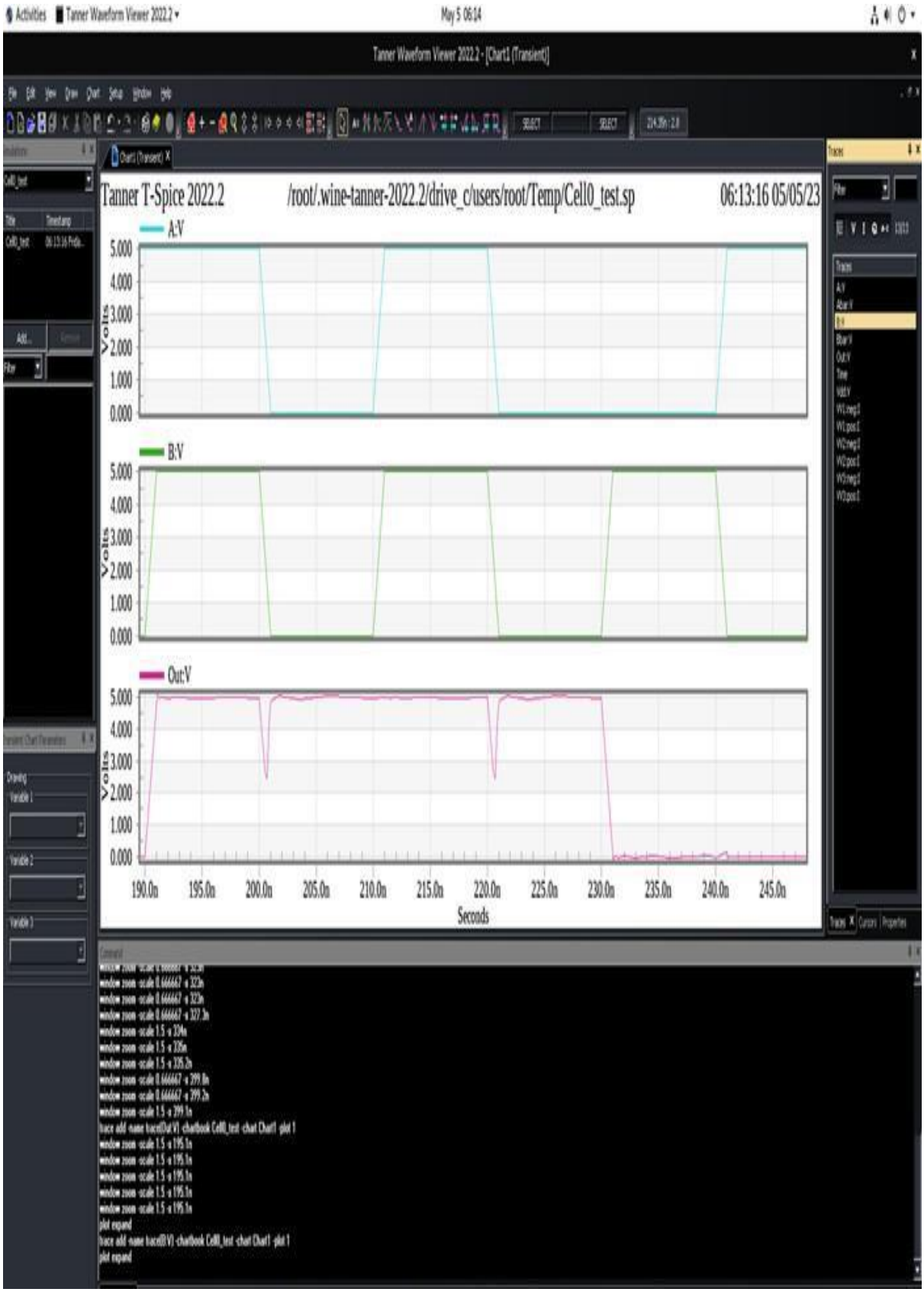
4.4. XNOR CIRCUIT



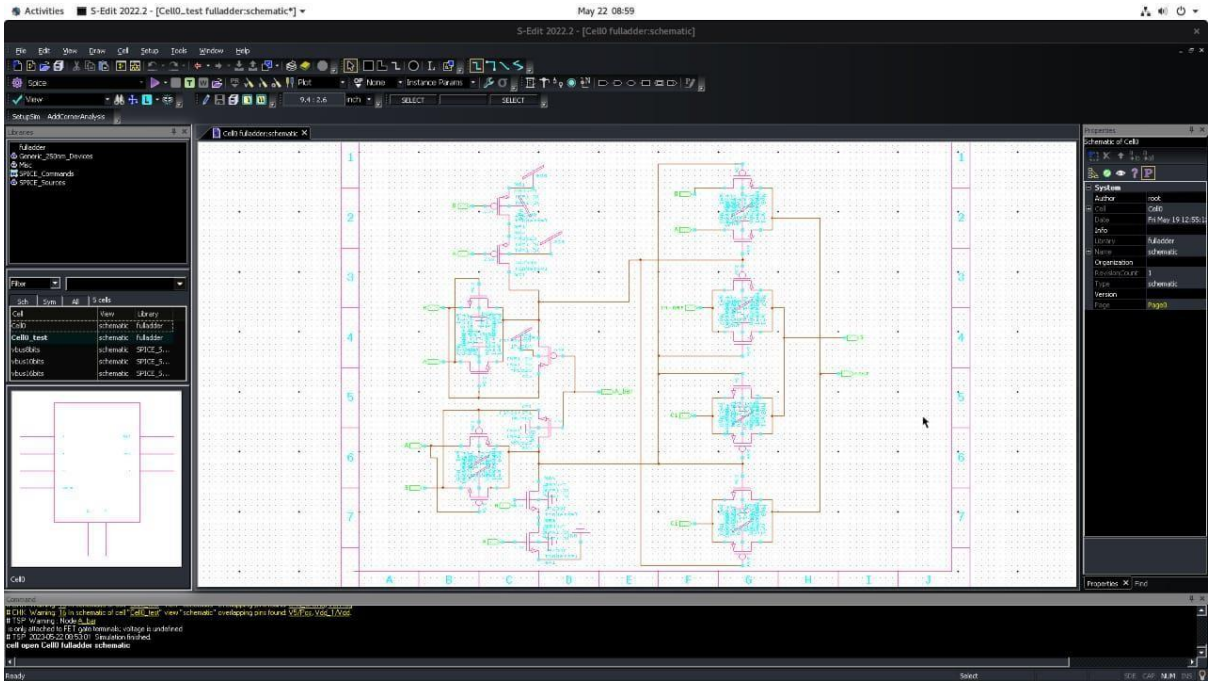
4.5. XNOR IC



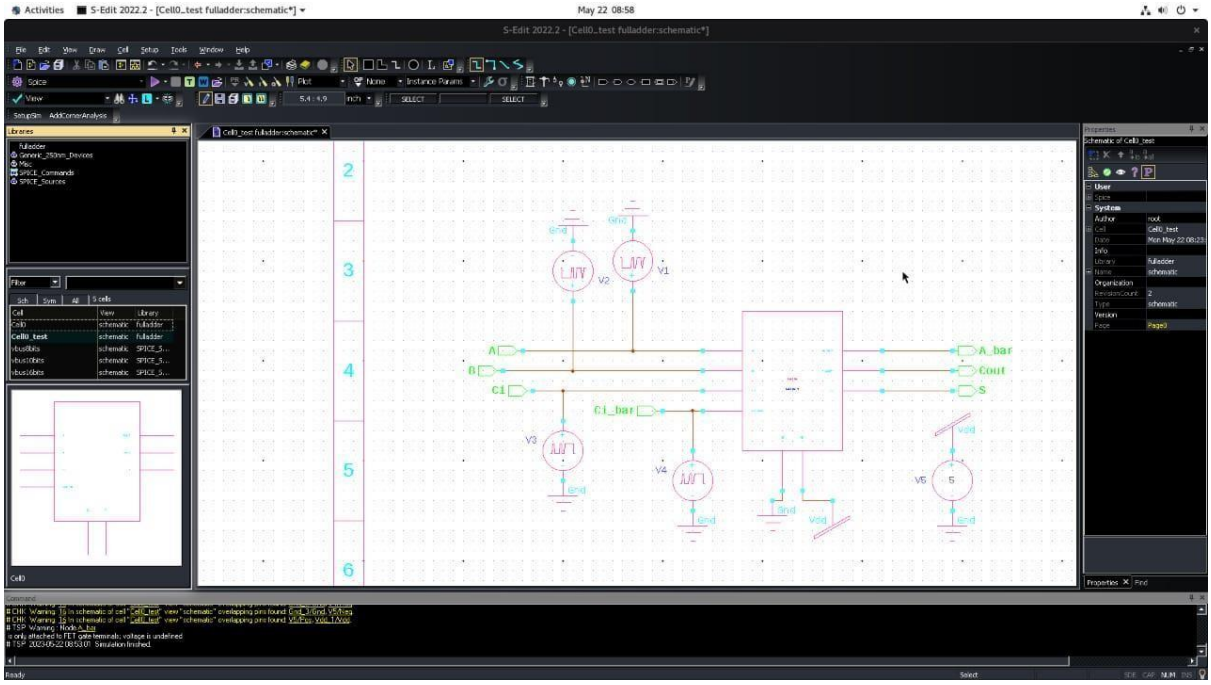
4.6. XNOR WAVEFORM



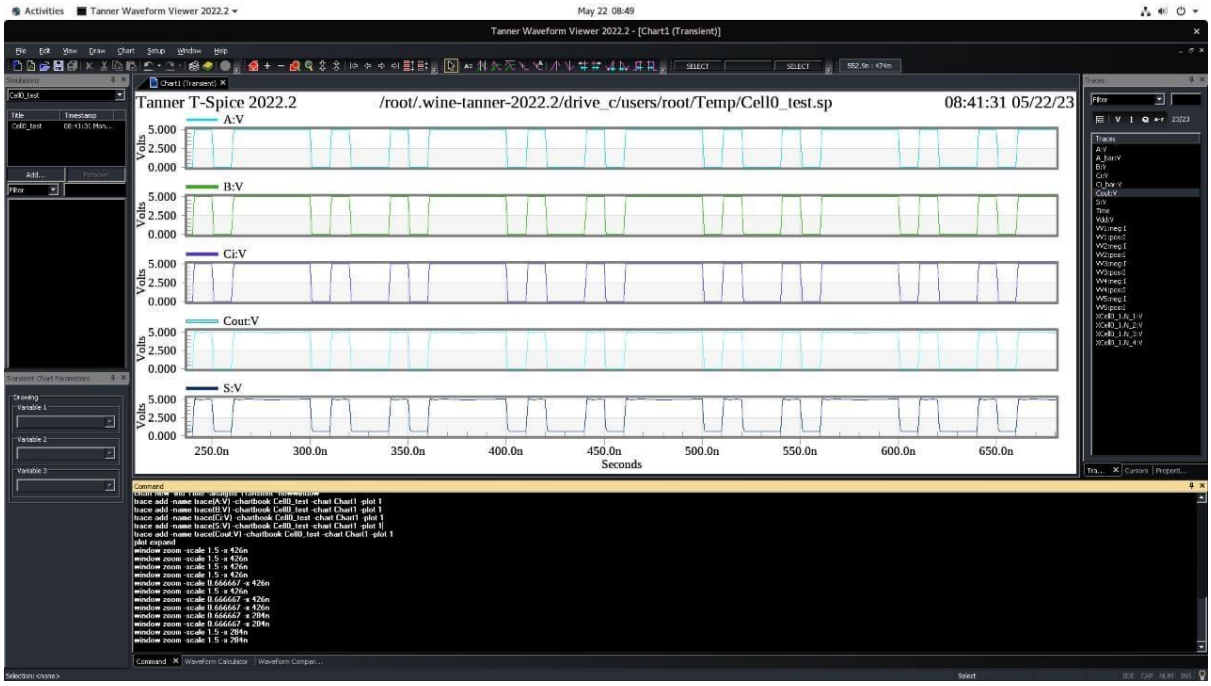
4.7. FULL ADDER CIRCUIT



4.8. FULL ADDER IC



4.9. FULL ADDER WAVEFORM



5.CONCLUSION

To conclude, we first evaluated the XOR/XNOR circuits. The evaluation revealed that using the NOT gates on the critical path of a circuit is a drawback. Another disadvantage of a circuit is to have a positive feedback on the outputs of the XOR–XNOR gate for compensating the output voltage level. This feedback increases the delay, output capacitance, and, as a result, energy consumption of the circuit. Then, we proposed new XOR/XNOR gates that do not have the mentioned disadvantages.

Finally, by using the proposed XOR/XNOR gates, we offered six new Full Adder cells for various applications. Also, a modified method for transistor sizing in digital circuits was proposed. The new method utilizes the numerical computation PSO algorithm to select the appropriate size for transistors on a circuit and also it has very good speed, accuracy, and convergence. After simulating the Full Adder cells in different conditions, the results demonstrated

that the proposed circuits have a very good performance in all simulated conditions.

Simulation results show that the proposed HFA-22T cell saves PDP and EDP, compared with its best counterpart. Also, this cell has better speed and energy at all supply voltages ranging from 0.65 to 1.5 V when is compared with other FA cells. The proposed HFA-22T has superior speed and energy against other FA designs at all different process corners. All proposed FAs have normal sensitivity to PVT variations.

5.1 FUTURE SCOPE

High-performance computing: As the demand for faster and more efficient computing continues to grow, it can play a significant role in improving the performance of arithmetic circuits. Future developments may focus on enhancing the speed and scalability of these adders to meet the requirements of emerging applications in areas like artificial intelligence, machine learning, and data analytics.

Low-power and energy-efficient designs: Power consumption is a critical concern in modern digital systems. Future research may explore techniques to reduce power consumption by optimizing the design at both the circuit and architectural levels. This could involve novel approaches to minimize switching activity, improve energy efficiency, and integrate power management techniques into these adder architectures.

HPC(High Performance Computing) systems, used in scientific research, data analysis, and simulations, can benefit from the incorporation of low-power and fast adders. These adders can contribute to overall energy savings and improved computational performance in large-scale computing environments.

The demand for energy-efficient processors in smartphones, tablets, and other mobile devices continues to rise. By incorporating low-power and fast

adders into the design of mobile processors, battery life can be extended, leading to longer usage times and enhanced user experience.

The use of low-power and fast adders can significantly impact the design of ICs, such as microprocessors and digital signal processors (DSPs). These adders can enhance the overall performance and energy efficiency of these circuits.

Department of Electronics and Communication Engineering

Vision

To be recognized by the society at large as a full- fledged department, offering quality higher education in the Electronics and Communication Engineering field with research focus catering to the needs of the stakeholders and staying in tune with the advancing technological revolution and cultural changes.

Mission

To achieve the vision, the department will

- Establish a unique learning environment to enable the students to face the challenges in Electronics and Communication Engineering field.
- Promote the establishment of centres of excellence in niche technology areas to nurture the spirit of innovation and creativity among faculty and students.
- Provide ethical and value-based education by promoting activities addressing the societal needs.
- Enable students to develop skills to solve complex technological problems and provide a framework for promoting collaborative and multidisciplinary activities.