SONA COLLEGE OF TECHNOLOGY, SALEM-5

(An Autonomous Institution)

M.E- VLSI Design

(Dept of ECE)

CURRICULUM and SYLLABI

[For students admitted in 2024-2025]

PG Regulations 2023

Approved by BOS and Academic Council meetings

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for M.E/M.Tech. Semester I under Regulations 2023 (CBCS)
Branch: VLSI Design

S.No	Course Code	Course Title	L	T	P	J	C	Category	Total Contact Hours	Course Type
	Theory Courses									
1.	P23MAT101B	Graph Theory and Combinatorics	3	0	0	0	3	FC	45	T
2.	P23VLD101	Advanced Digital System Design	3	1	0	0	4	PC	60	TT
3.	P23VLD102	CMOS Digital VLSI Design	3	0	0	0	3	PC	45	T
4.	P23VLD103	Solid State Device Modeling and Simulation	3	0	0	0	3	PC	45	T
5.	P23VLD104	VLSI Signal Processing	3	0	0	0	3	PC	45	T
6.	P23GE101	Research Methodology and IPR	3	0	0	0	3	PC	45	T
7.	P23GE702	Audit Course: Stress Management by Yoga	2	0	0	0	0	AC	30	T
	Practical Courses									
8.	P23VLD105	VLSI Design Laboratory	0	0	2	0	1	PC	30	L
		Total Credits					20			

Approved By

Chairperson, ECE BoS	Member Secretary, Academic Council	Dean-Academics	Chairperson, Academic Council & Principal
Dr.R.S.Sabeenian	Dr.R.Shivakumar	Dr.J.Akilandeswari	Dr.S.R.R.Senthil Kumar

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Copy to:-
HOD/ ECE, First Semester M.E.(VLSI Design) Students and Staff, COE

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for M.E/M.Tech. Semester II under Regulations 2023 (CBCS)
Branch: VLSI Design

S.No	Course Code	Course Title	L	T	P	J	C	Category	Total Contact Hours	Course Type*
Theory courses										
1.	P23VLD201	Low Power VLSI Design	2	0	0	2	3	PC	60	TP
2.	P23VLD202	Embedded C++	3	0	0	0	3	PC	45	T
3.	P23VLD203	Design for Testability	2	0	0	2	3	PC	60	TP
4.	P23VLD504	**Elective:** CAD of VLSI Circuits	3	0	0	0	3	PC	45	T
5.	P23VLD505	**Elective:** Computer Architecture and Parallel processing	3	0	0	0	3	PC	45	T
6.	P23VLD506	**Elective:** Image Analysis and Computer Vision	3	0	0	0	3	PC	45	T
7.	P23GE701	**Audit Course** – English for Research Paper Writing	2	0	0	0	0	AC	30	T
Practical courses										
8.	P23VLD204	VLSI Design and Testing Laboratory	0	0	2	0	1	PC	30	L
9.	P23VLD205	Mini Project	0	0	0	2	1	PC	30	P
Total Credits							**20**			

*T- Theory, TT- Theory with Tutorial, TL- Theory with Laboratory, TP -Theory with Project, TLP- Theory with Laboratory and Project, L-Laboratory, LT- Laboratory with Theory, LP- Laboratory with Project,P-Project

Approved By

Chairperson -- BoS	**Member Secretary/ Academic Council**	**Dean-Academics**	**Chairperson, Academic Council & Principal**
Dr.R.S.Sabeenian	**Dr.R.Shivakumar**	**Dr.J.Akilandeswari**	**Dr.S.R.R.Senthil Kumar**

Copy to:-HOD/ ECE, Second Semester ME VLSI Students and Staff, COE

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for M.E/M.Tech. Semester III under Regulations 2023 (CBCS)
Branch: VLSI Design

S.No	Course Code	Course Title	L	T	P	J	C	Category	Total Contact Hours	Course Type*
Theory courses										
1.	**P23VLD503**	**Elective:** ASIC Design	3	0	0	0	3	PE	45	T
2.	**P23VLD507**	**Elective:** Nano Electronics	3	0	0	0	3	PE	45	T
3.	**P23VLD516**	**Elective:** Analysis and Design of Digital Integrated Circuits	3	0	0	0	3	PE	45	T
4.	**P23VLD301**	Project Work-I	0	0	0	16	8	PC	240	P
Total Credits							**17**			

*T- Theory, TT- Theory with Tutorial, TL- Theory with Laboratory, TP- Theory with Project, TLP- Theory with Laboratory and Project, L-Laboratory, LT- Laboratory with Theory, LP- Laboratory with Project ,P-Project

Approved By

14/6/25	20/6/25	20/6/25	
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Copy to:
HOD/ ECE, Third Semester ME VLSI Students and Staff, COE

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for M.E/M.Tech. Semester IV under Regulations 2023 (CBCS)
Branch: VLSI Design

S.No	Course Code	Course Title	L	T	P	J	C	Category	Total Contact Hours	Course Type*
Practical courses										
1.	P23VLD401	Project Work-II	0	0	0	28	14	PC	420	P
						Total Credits	**14**			

*T- Theory, TT- Theory with Tutorial, TL- Theory with Laboratory, TP- Theory with Project, TLP- Theory with Laboratory and Project, L-Laboratory, LT- Laboratory with Theory, LP- Laboratory with Project

Approved By

12/12/2025			
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Copy to:- HOD/ Electronics and Communication Engineering, Fourth Semester M.E VLSI Students and Staff, COE

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for M.E/M.Tech. Semester I under Regulations 2023 (CBCS)
Branch: VLSI Design

S.No	Course Code	Course Title	L	T	P	J	C	Category	Total Contact Hours	Course Type
	Theory Courses									
1.	P23MAT101B	Graph Theory and Combinatorics	3	0	0	0	3	FC	45	T
2.	P23VLD101	Advanced Digital System Design	3	1	0	0	4	PC	60	TT
3.	P23VLD102	CMOS Digital VLSI Design	3	0	0	0	3	PC	45	T
4.	P23VLD103	Solid State Device Modeling and Simulation	3	0	0	0	3	PC	45	T
5.	P23VLD104	VLSI Signal Processing	3	0	0	0	3	PC	45	T
6.	P23GE101	Research Methodology and IPR	3	0	0	0	3	PC	45	T
7.	P23GE702	Audit Course: Stress Management by Yoga	2	0	0	0	0	AC	30	T
	Practical Courses									
8.	P23VLD105	VLSI Design Laboratory	0	0	2	0	1	PC	30	L
		Total Credits					20			

Approved By

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Copy to:-
HOD/ ECE, First Semester M.E.(VLSI Design) Students and Staff, COE

ELECTRONICS AND COMMUNICATION ENGINEERING						
M. E. / VLSI DESIGN						
SEMESTER - I	GRAPH THEORY AND COMBINATORICS	L	T	P	J	C
P23MAT101B		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	apply the counting principles to the real world problems.
CO2:	solve the homogeneous and nonhomogeneous recurrence relations by the method of substitution and generating functions.
CO3:	find the shortest path and minimal spanning tree of a weighted graph through algorithms.
CO4:	find the matching and connectivity of a graph.
CO5:	apply the concepts of planarity and coloring of a graph in a network problem.

Pre-requisites:

- Basics of elementary algebra
- Basics of calculus
- Basics of geometry
- Basics of discrete mathematics

CO/PO, PSO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcomes (PSOs)				
	PO1	PO2	PO3	PO4	PO5
CO1	3	3	2	3	3
CO2	3	3	2	3	3
CO3	3	3	2	3	3
CO4	3	3	2	3	3
CO5	3	3	2	3	3

Course assessment methods [Theory]

Direct		Indirect
CIE test I (10) (Theory) CIE test II (10) (Theory) CIE test III (10) (Theory) Assignment / Problem- solving / Seminar (10)	Total CIE: 40 marks Semester End Examination: 60 marks	Course end survey

Unit 01	COMBINATORICS	9 Hours

Mathematical induction – basics of counting – permutations and combinations – enumeration of permutations and combinations with constrained repetitions – enumeration of permutations and combinations without constrained repetitions – principle of inclusion and exclusion.

Unit 02	RECURRENCE RELATIONS	9 Hours

Generating functions of sequences – calculating coefficients of generating functions – recurrence relations – solving recurrence relations by substitution and generating functions – method of characteristic roots – solutions of homogeneous and nonhomogeneous recurrence relations.

Unit 03	GRAPH THEORY	9 Hours
Fundamental concepts of graph – paths – cycles – trails – vertex degrees and counting – trees and distance – shortest path algorithm (Dijkstra's & Warshall's algorithm) – spanning trees – optimization and trees (Prim's & Kruskal's algorithm).		
Unit 04	**MATCHING AND CONNECTIVITY**	**9 Hours**
Matching and coverings – optimal assignment problem – travelling salesman problem – vertex and edge connectivity – network flow problems.		
Unit 05	**COLORING AND PLANAR GRAPHS**	**9 Hours**
Vertex coloring – edge coloring – chromatic polynomial – color critical graphs – planar graphs – duality – Euler's formula – characterization of planar graphs – parameters of planarity.		

Theory: 45 Hrs	Tutorial: -	Practical:	Project:–	Total Hours: 45 Hrs

TEXT BOOK:

1.	D. B. West, "Introduction to Graph Theory", Pearson Publishers, 2nd Edition, 2017.

REFERENCE BOOKS:

1.	N. Deo, "Graph Theory with Applications to Engineering and Computer Science", Dover Publishers, 1st Edition, 2016.
2.	J. L. Mott, A. Kandel and T. P. Baker, "Discrete mathematics for Computer Scientists and Mathematics", Brady Publishers, 2nd Edition, 1985.
3.	R. J. Wilson, "Introduction to Graph Theory", Pearson Publishers, 4th Edition, 2009.
4.	R. Balakrishnan and K. Ranganathan, "A Textbook of Graph Theory", Springer Publishers, 2nd Edition, 2012.
5.	V. K. Balakrishnan, "Graph Theory", Mc Graw Hill Publishers, 1st Edition, 2004.

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BoS – Chairperson / Science and Humanities

P23VLD101	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	J	C
		3	1	0	0	4

Course Outcomes

At the end of the course, the student will be able to

CO1:	Design and analyze the synchronous sequential circuits.
CO2:	Analyze synchronous sequential circuits using ASM.
CO3:	Design and analyze asynchronous sequential circuits.
CO4:	Design synchronous sequential circuit using programmable devices.
CO5:	Synthesize digital circuit using Verilog HDL.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	1	1	1	3	3
CO2	1	1	2	3	3
CO3	2	1	2	3	3
CO4	2	1	2	3	3
CO5	2	1	2	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN	12 Hours

Structure and Operation of Clocked Synchronous Sequential Networks – Analysis of Clocked Synchronous Sequential Circuits – Modeling of Clocked Synchronous Sequential Network Behavior – Serial Binary Adder Using Mealy and Moore Networks – Sequence Recognizer – State Table Reduction – State Assignment – Design of Clocked Synchronous Sequential Circuits.

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Unit 02: SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN USING ASM	12 Hours
Algorithmic State Machine – ASM Charts – ASM Blocks – Sequence Recognition Using ASM Charts – State Assignments – ASM Transition Tables – ASM Excitation Tables – ASM Realization Using Discrete Gates – Multiplexers – Design of Iterative Circuits.	
Unit 03: ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN	**12 Hours**
Structure and Operation of Asynchronous Sequential Networks – Analysis of Asynchronous Sequential Circuit – Races and Hazards in Asynchronous Sequential Networks – Primitive Flow Table – Reduction of Input Restricted Flow Tables – Flow Table Reduction – State Assignment Problem and the Transition Table - Design of Asynchronous Sequential Circuits.	
Unit 04: SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES	**12 Hours**
Programming logic device families – PLAs – PROMs – Designing a synchronous sequential circuit using PLA/PAL. Realization of finite state machine using PLD – CPLD - FPGA – Xilinx FPGA - Xilinx 4000 – Altera MAX 5000 and 7000 – Altera MAX 9000.	
Unit 05: SYSTEM DESIGN USING VERILOG	**12 Hours**
Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines – Structural modeling – Compilation and Simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – Sequential machine – Serial adder – Multiplier- Divider – Design of simple microprocessor.	

Theory: 45 Hrs	Tutorial: 15Hrs	Practical: 0	Project: 0	Total Hours: 60 Hrs

REFERENCES

1. Donald G. Givone, "*Digital principles and Design*", Tata McGraw Hill, 2017.
2. J. Bhasker, "*A Verilog HDL Primer*", BS Publications, 3rd edition, 2023.
3. William I. Fletcher, "*An Engineering Approach to Digital Design*", Prentice Hall India, 2009.
4. Charles H. Roth Jr.,"*Fundamentals of Logic design*", Thomson Learning, 2005.
5. Nripendra N. Biswas, "*Logic Design Theory*", Prentice Hall of India, 2005.

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P23VLD102	CMOS DIGITAL VLSI DESIGN	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Illustrate the VLSI design and fabrication processes of MOSFETs.
CO2:	Describe and evaluate the MOSFET operations and modeling of MOSFETS.
CO3:	Analyze and evaluate the static and switching characteristics of CMOS inverters.
CO4:	Design combinational and sequential logic circuits using CMOS principles
CO5:	Analyze tradeoffs of the various circuit choices for each of the building block.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	1	2	1	3	3
CO2	1	2	2	3	3
CO3	1	2	3	3	3
CO4	1	2	3	3	3
CO5	1	2	3	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: INTRODUCTION AND FABRICATION OF MOSFETS — **9 Hours**

Overview of VLSI Design Methodologies – VLSI Design Flow – Design Hierarchy – Concepts of Regularity, Modularity and Locality – VLSI Design Styles – Design Quality – Packaging Technology – Fabrication Process Flow Basic Steps – The CMOS n-Well Process – Layout Design Rules – Full-Custom Mask Layout Design.

4/8/23

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Unit 02: MOS TRANSISTORS AND IT'S MODELING USING SPICE	9 Hours
The MOS Structure – The MOS System under External Bias – Structure and Operation of MOS Transistor –Current-Voltage Characteristics –Scaling and Small -Geometry Effects –Capacitances – Basic Concepts of Modeling of MOS –The LEVEL 1 Model Equations – The LEVEL 2 Model Equations – The LEVEL 3 Model Equations – State-of-the-Art MOSFET Models – Capacitance Models – Comparison of the SPICE MOSFET Models.	
Unit 03: MOS INVERTERS AND CHARACTERISTICS	**9 Hours**
Static Characteristics of Resistive Load Inverter – Inverters with n-Type MOSFET Load – CMOS Inverter – Introduction of Switching Characteristics – Delay Time – Determination of delay Times – Inverter Design with Delay Constraints – Estimation of Interconnect Parasitic – Calculation of Interconnect Delay – Switching power Dissipation of CMOS inverters.	
Unit 04: COMBINATIONAL AND SEQUENTIAL CMOS LOGIC CIRCUITS	**9 Hours**
MOS Logic Circuits with Depletion nMOS Loads – CMOS Logic Circuits – Complex Logic Circuits – Transmission Gates – Behavior of Bistable Elements – CMOS SR Latch Circuit – Clocked Latch and Flip – Flop Circuits –D-Latch and Edge-Triggered Flip-Flop.	
Unit 05: ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES	**9 Hours**
Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.	

Theory: 45 Hrs	Tutorial: 0	Practical: 0	Project: 0	Total Hours: 45 Hrs

REFERENCES

1.	Anantha P. Chandrakasan, Borivoje Nikolic, and Jan M. Rabaey , "Digital Integrated Circuits: A Design Perspective", Pearson Education, 2003.
2.	Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis and Design", McGraw Hill Education (India) Pvt. Ltd., 3rd Edition, 2019
3.	Bhaskar J., "A Verilog HDL Primer", B. S. Publications, 2nd Edition, 2018.
4.	Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design - A System Perspective", Pearson Education ASIA, 2nd Edition, 2010
5.	R. Jacob Baker, "CMOS circuit design, Layout, and Simulation", John Wiley and Sons, 2012.

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P23VLD103	SOLID STATE DEVICE MODELING AND SIMULATION	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Analyze the concepts and procedural flow that are used to construct the complicated device models.
CO2:	Analyze the design challenges involved in device models.
CO3:	Analyze the noise models of MOSFET.
CO4:	Analyze the EKV and BSIM4 MOSFET models.
CO5:	Analyze the modeling of passive devices and process variation

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2	1	2	3	3
CO2	2	1	2	3	3
CO3	2	1	2	3	3
CO4	2	1	2	3	3
CO5	2	1	2	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: MOSFET DEVICE PHYSICS	9 Hours

Introduction to solids, Bonding forces and energy bands in solid semiconductors, MOS capacitor - Interface Charge, threshold voltage, MOS Capacitance, MOS Charge control model, MOS Operation and characteristics. MOSFET fabrication process.

24/9/25

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Unit 02: MOSFET MODELING	9 Hours
Basic MOSFET Modeling-Meyer model, velocity saturation model, capacitance model, Basic small signal model. Advanced MOSFET Modeling- modeling approach, High field effects, short channel effects, Gate leakage and effective oxide thickness, Unified MOSFET C–V Model- Unified Meyer C–V model, Ward–Dutton model, Non-quasi-static modeling.	
Unit 03: NOISE MODELING	**9 Hours**
Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, modeling for accurate distortion analysis-nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit.	
Unit 04: BSIM4 MOSFET MODELING	**9 Hours**
Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, Mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, Noise model, Junction diode models , Layout-dependent parasities model. The EKV model.	
Unit 05: MODELING OF PASSIVE DEVICES AND PROCESS VARIATION	**9 Hours**
Introduction – Resistors – Well Resistor – Metal Resistor – Diffused Resistor – Poly Resistor – Capacitors – Poly-Poly Capacitors – Metal-Insulator-Metal Capacitors – MOSFET Capacitors – Junction Capacitors – Inductors – The Influence of Process Variation and Device Mismatch.	

Theory: 45 Hrs	Tutorial: 0	Practical: 0	Project: 0	Total Hours: 45 Hrs

REFERENCES

1.	TrondYtterdal, Yuhua Cheng and Tor A. Fjeldly, "*Device Modeling for Analog and RF CMOS Circuit Design*", John Wiley &1 edition, 2008.
2.	Grasser, T., "Advanced Device Modeling and Simulation ", World Scientific Publishing Company, 2008.
3.	Ben G. Streetman, "Solid State Devices", Prentice Hall, 2015.
4.	Carlos Galup-Montoro, Marco Cherem Schneider, "MOSFET Modeling for Circuit Analysis and Design", World Scientific Publishing Co. Pte. Ltd., 2007.
5.	Rudan, Massimo, "Physics of Semiconductor Devices", Springer International Publishing, 2017.

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P23VLD104	VLSI SIGNAL PROCESSING	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Discuss about the introduction of DSP systems, pipelining and parallel processing.
CO2:	Analyze the different techniques of retiming, folding and unfolding
CO3:	Explain the different algorithms used for fast convolution, pipelining, parallel and processing of IIR filters
CO4:	Design the different types of multipliers and CSD Representation of VLSI systems.
CO5:	Discuss about the synchronous and asynchronous pipelining and need for low power VLSI

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	3	3
CO2	1	1	3	3	3
CO3	1	1	3	3	3
CO4	3	1	3	3	3
CO5	1	1	3	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: INTRODUCTION TO DSP SYSTEMS — **9 Hours**

Introduction to DSP Systems – Typical DSP Algorithms – Iteration Bound – Data Flow Graph Representations – Loop Bound and Iteration Bound – Algorithms for Computing Iteration Bound – Pipelining and Parallel Processing – Pipelining of FIR Digital Filters – Parallel Processing – Pipelining and Parallel Processing for Low Power

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Unit 02: RETIMING, FOLDING AND UNFOLDING	9 Hours
Retiming – Definitions and Properties – Retiming Techniques – Unfolding –Properties of Unfolding –Applications – Sampling Period Reduction – Parallel Processing –Folding – Folding Transformation – Register Minimizing Techniques – Register Minimization in Folded Architectures.	
Unit 03: FAST CONVOLUTION	**9 Hours**
Fast Convolution – Cook-Toom Algorithm – Iterated Convolution – Cyclic Convolution – Pipelined and Parallel Recursive and Adaptive Filters – Pipeline Interleaving in Digital Filters – Pipelining in First Order IIR Filters – Parallel Processing for IIR Filters – Combined Pipelining and Parallel Processing for IIR Filters – Pipelined Adaptive Digital Filters – Relaxed Look-Ahead – Pipelined LMS Adaptive Filter.	
Unit 04: BIT-LEVEL ARITHMETIC ARCHITECTURES	**9 Hours**
Bit-Level Arithmetic Architectures – Parallel Multipliers – Baugh-Wooley Multipliers – Interleaved Floor - Plan and Bit-Plane – Based Digital Filters – Design of Lyon's Bit-Serial Multipliers using Horner's Rule – Bit Serial FIR Filter – CSD Representation – CSD Multiplication using Horner's Rule for Precision Improvement – Distributed Arithmetic	
Unit 05: SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING	**9 Hours**
Synchronous – Wave and Asynchronous Pipelining – Synchronous Pipelining and Clocking Styles – Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs –Wave Pipelining – Asynchronous Pipelining – Programming Digital Signal Processors – General Architecture with Important Features.	

Theory: 45 Hrs	Tutorial: 0	Practical: 0	Project: 0	Total Hours: 45 Hrs

REFERENCES

1.	Keshab K. Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2.	Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
3.	S.Y.kung, H.J.White house, T. Kailath," VLSI and Modern Signal Processing", Prentice hall,
4.	R.G. Lyons, Understanding Digital Signal Processing, Pearson Education, 2004

4/8/23

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P23VLD105	VLSI DESIGN LABORATORY	L	T	P	J	C
		0	0	2	0	1

Course Outcomes

At the end of the course, the student will be able to

CO1:	Design and analysis of the digital systems using Verilog HDL
CO2:	Implement the digital system design in the FPGA Board and analyse the same for performance
CO3:	Design the NMOS, and CMOS Logic circuits and analyse the characteristics of the same

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2		3	3	3
CO2	2		3	3	3
CO3	2		3	3	3

Course Assessment methods

Direct		Indirect
CIE test I (20) Quiz 1 (5) CIE test II (20) Quiz 2 (5)	RTPS (10) Total CIE: **60 marks** Semester End Examination: **40 marks**	Course end survey

List of Experiments

1. Design of NMOS and CMOS Inverters - DC and transient characteristics and switching times
2. Design of CMOS logic gate circuits
   i) Static Logic
   ii) Dynamic Logic
   iii) Domino Logic
3. Design of combinational circuits using Verilog and implement in FPGA.
   i) Multiplexer and De-Multiplexer
   ii) Encoder and Decoder
   iii) Comparator
4. Design of sequential circuits using Verilog and implement in FPGA
   i) Shift Registers
   ii) Counters
5. Design and implementation of ALU using FPGA and Verilog HDL.

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6. Design of FIR filters CORDIC using FPGA and Verilog HDL.
7. Design and implementation of floating-point multiplier
8. Design and implementation of Stepper Motor using FPGA
9. Design and implementation of traffic controller using FPGA

Theory: 0	Tutorial: 0	Practical: 30 Hrs	Project: 0	Total Hours: 30 Hrs

4/8/25

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P23GE101 **RESEARCH METHODOLOGY AND IPR** 3 0 0 0 3

(Common to all M.E /M.Tech Programmes)

COURSE OUTCOMES:

At the end of the course, the student will be able to

1. Review the literature of the research problem
2. Choose appropriate data collection and sampling method according to the research problem.
3. Interpret the results of research and communicate effectively with their peers
4. Explain the Importance of intellectual property rights
5. Evaluate trade mark, develop and register patents.

CO/PO, PSO Mapping (3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak COs Programme Outcomes (POs) and Programme Specific Outcomes (PSOs)					
COs	PO1	PO2	PO3	PO4	PO5
CO1	2	3	3	3	3
CO2	2	3	3	3	3
CO3	2	3	3	3	3
CO4	2	3	3	3	3
CO5	3	3	3	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) (Theory) CIE test II (10) (Theory) CIE test III (10) (Theory)	Assignment / Problem –Solving /Seminar (10) Total CIE: **40 Marks** Semester End Examination : **60 Marks**	Course end survey

UNIT I INTRODUCTION TO RESEARCH METHODS 9

Definition and Objective of Research, Various steps in Scientific Research, Types of Research, Criteria for Good Research, Defining Research Problem, Research Design , Case Study Collection of Primary and Secondary Data, Collection Methods: Observation, Interview, Questionnaires, Schedules,

UNIT II SAMPLING DESIGN AND HYPOTHESIS TESTING 9

steps in Sampling Design, Types of Sample Designs, Measurements and Scaling Techniques -Testing of hypotheses concerning means (one mean and difference between two means -one tailed and two tailed tests), concerning variance — one tailed Chi-square test.

UNIT II INTERPRETATION AND REPORT WRITING 9

Techniques of Interpretation, Precaution in Interpretation, Layout of Research Report, Types of Reports, Oral Presentation, Mechanics of Writing Research Report

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY 9

Introduction, types of intellectual property, international organizations, agencies and treaties, importance of intellectual property rights, Innovations and Inventions trade related intellectual property rights.

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UNIT V TRADE MARKS, COPY RIGHTS AND PATENTS 9

Purpose and function of trade marks, acquisition of trade mark rights, trade mark registration processes, trademark claims —trademark Litigations- International trademark law Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law. Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer

Lecture: 45, Tutorial: 0, Total: 45 Hours

TEXT BOOKS

1. C.R. Kothari, Gaurav Garg, Research Methodology Methods and Techniques An Edition, New Age International Publishers, 2019.
2. Deborah E. Bouchoux, "Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets", Delmar Cengage Learning, 4" Edition, 2012.
3. Prabuddha Ganguli, "Intellectual Property Rights: Unleashing the Knowledge Economy", Tata Mc Graw Hill Education, 1" Edition, 2008.

REFERENCE BOOKS

1. Panneerselvam, R., Research Methodology, Second Edition, Prentice-Hall of India, New Delhi, 2013.
2. Ranjith Kumar, Research Methodology — A step by step Guide for Begineers, 4" edition, Sage publisher, 2014.
3. D Llewelyn & T Aplin W Cornish, "Intellectual Property: Patents, Copyright, Trade Marks and Allied Rights", Sweet and Maxwell, 1" Edition, 2016.
4. Ananth Padmanabhan, "Intellectual Property Rights-Infringement and Remedies", Lexis Nexis, 1" Edition, 2012.
5. Ramakrishna B and Anil Kumar H.S, "Fundamentals of Intellectual Property Rights: For Students, Industrialist and Patent Lawyers", Notion Press, 1" Edition, 2017.
6. M.Ashok Kumar and Mohd. Iqbal Ali :"Intellectual Property Rights" Serials Pub

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P23GE702	Stress Management by Yoga	L	T	P	J	C
		2	0	0	0	0

Course Outcomes

At the end of the course, the student will be able to

CO1:	Develop physical and mental health thus improving social health
CO2:	Increase immunity power of the body and prevent diseases
CO3:	Accelerate memory power
CO4:	Achieve the set goal with confidence and determination
CO5:	Improve stability of mind, pleasing personality and work with awakened wisdom

Course Assessment methods

Direct		Indirect
CIE test I (30) CIE test II (30) CIE test III (40)	Total CIE: 100 marks Semester End Examination: NIL	Course end survey

Unit 01: **6 Hours**

Yoga-Introduction - Astanga Yoga- 8 parts-Yam and Niyam etc.- Do's and Don'ts in life-Benefits of Yoga and Asana- Yoga Exercise- and benefits- Pranayam Yoga- Nadi suthi, Practice and Spinal Sclearance Practice-Regularization of breathing techniques and its effects-Practice and kapalapathy practice.

Unit 02: **6 Hours**

Neuromuscular breathing exercise and Practice- Magarasa Yoga, 14 points Acupressure techniques and practice-Body relaxation practice and its benefits- Raja Yoga- 1.Agna –explanation and practice- Activation of Pituitary- Raja Yoga- 2. Santhi Yoga-Practice-Balancing of physical and mental power.

Unit 03: **6 Hours**

Raja Yoga- 3. Sagasrathara yoga –practice- Activation of dormant brain cells-Kayakalpa-theory- Kayakalpa –practice-Yogic exercise to improve physical and mental health and practice-Asanas –explanation-Practice-benefits

Unit 04: **6 Hours**

Sun namaskar- 12 poses-explanation and practice-Yoga –Asana-Padmasana, vajrasana,chakrasana, viruchasana etc-Stress management with Yoga-Role of women and Yoga Equality, nonviolence, Humanity, Self- control- Food and yoga Aware of self-destructive habits Avoid fault thinking (thought analysis-Practice)-Yoga Free from ANGER (Neutralization of anger)& practice

Unit 05: **6 Hours**

Moralisation of Desire & practice- Punctuality-Love-Kindness-Compassion Eradication of worries-Practice - Personality development, positive thinking-Good characters to lead a moral life How to clear the polluted mind- Benefits of blessing- Five- fold culture –explanation- Karma Yoga Practice In Geetha- Sense of duty-Devotion, self- reliance, confidence, concentration, truthfulness, cleanliness.

Theory: 30 Hrs	Tutorial: --	Practical: --	Project:--	Total Hours: 30 Hrs

REFERENCES

1	'Yogic Asanas for Group Tarining-Part-I" Janardan Swami Yogabhyasi Mandal, Nagpur
2	"Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata

HOD
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Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for M.E/M.Tech. Semester II under Regulations 2023 (CBCS)
Branch: VLSI Design

S.No	Course Code	Course Title	L	T	P	J	C	Category	Total Contact Hours	Course Type*
Theory courses										
1.	P23VLD201	Low Power VLSI Design	2	0	0	2	3	PC	60	TP
2.	P23VLD202	Embedded C++	3	0	0	0	3	PC	45	T
3.	P23VLD203	Design for Testability	2	0	0	2	3	PC	60	TP
4.	P23VLD504	**Elective:** CAD of VLSI Circuits	3	0	0	0	3	PC	45	T
5.	P23VLD505	**Elective:** Computer Architecture and Parallel processing	3	0	0	0	3	PC	45	T
6.	P23VLD506	**Elective:** Image Analysis and Computer Vision	3	0	0	0	3	PC	45	T
7.	P23GE701	**Audit Course** – English for Research Paper Writing	2	0	0	0	0	AC	30	T
Practical courses										
8.	P23VLD204	VLSI Design and Testing Laboratory	0	0	2	0	1	PC	30	L
9.	P23VLD205	Mini Project	0	0	0	2	1	PC	30	P
Total Credits							**20**			

*T- Theory, TT- Theory with Tutorial, TL- Theory with Laboratory, TP -Theory with Project, TLP- Theory with Laboratory and Project, L-Laboratory, LT- Laboratory with Theory, LP- Laboratory with Project,P-Project

Approved By

Chairperson -- BoS	**Member Secretary/ Academic Council**	**Dean-Academics**	**Chairperson, Academic Council & Principal**
Dr.R.S.Sabeenian	**Dr.R.Shivakumar**	**Dr.J.Akilandeswari**	**Dr.S.R.R.Senthil Kumar**

Copy to:-HOD/ ECE, Second Semester ME VLSI Students and Staff, COE

P23VLD201	LOW POWER VLSI DESIGN	L	T	P	J	C
		2	0	0	2	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Evaluate about the sources of power consumption in CMOS and hierarchy of limits
CO2:	Estimate the power in CMOS at logic level and circuit level.
CO3:	Analyze the synthesis and software design for low power.
CO4:	Analyze the SOI CMOS Devices.
CO5:	Design SOI CMOS digital and analog circuits.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2	1	2	3	3
CO2	2	1	2	3	3
CO3	2	1	2	3	3
CO4	2	1	2	3	3
CO5	2	1	2	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) - Theory CIE test II (10) – Theory CIE test III (10) – Theory CIE test IV(10) – Project	Assignment / Quiz/ Seminar (10) Total CIE: 50 marks Semester End Examination: 50 marks [SEE- Theory (25 marks), Project (25 marks)	Course end survey

Unit 01: POWER DISSIPATION IN CMOS — **6 Hours**

Introduction – Sources of Power Dissipation – Designing for Low power – Physics of Power Dissipation in MOSFET Devices – Power Dissipation in CMOS – Hierarchy of Limits of Power – Fundamental-Material- Device-Circuit and System limits.

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Unit 02: POWER ESTIMATION	6 Hours
Power Estimation Using Input Vector Compaction – Power Dissipation in Domino CMOS – Circuit Reliability – Power Estimation at the Circuit Level – High Level Power Estimation – Information-Theory-Based Approaches – Estimation of Maximum power.	
Unit 03: SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER	**6 Hours**
Behavioral Level Transforms – Logic Level Optimization for Low power – Circuit Level – Sources of Software Power Dissipation – Software Power Estimation – Software Power Optimizations – Automated Low-Power Code Generation – Co-design for Low Power.	
Unit 04: SOI CMOS DEVICE	**6 Hours**
Introduction – Basic SOI Technology – Back Gate Bias Effects – Short Channel Effects – Narrow Channel Effects – Mobility – Floating Body Effects – Subthreshold Behavior – Impact Ionization – Breakdown – Transient-Induced Leakage – Self-Heating – Hot Carriers – Accumulation-Mode Devices.	
Unit 05: SOI CMOS DIGITAL AND ANALOG CIRCUITS	**6 Hours**
Static and Dynamic Logic Circuits – DRAM – SRAM – CAM – Gate Array – CPU – Multiplier and DSP – Frequency Divider – SOI Op Amps – Filters – ADC and DAC – Sigma – Delta ADC – RF Circuits Sigma – Low Noise Amplifier – Mixer – Voltage Controlled Oscillator.	
Project:	**30 Hours**
During the project work, each student focuses on fundamental skills, laying the groundwork for advanced projects that integrate theoretical knowledge with practical applications in the Low Power VLSI Design Additionally, they improve their problem-solving abilities and cultivate teamwork skills essential for collaborative project development.	

Theory: 30 Hrs	Tutorial: --	Practical: --	Project: 30 Hrs	Total Hours: 60 Hrs

REFERENCES

1. Roy K. and Prasad S.C. *"Low Power CMOS VLSI circuit design,"* Wiley,2011.
2. James B. Kuo, Shin chia Lin, *"Low voltage SOI CMOS VLSI Devices and Circuits"*, John Wiley and sons, inc 2008.
3. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, *"Designing CMOS Circuits for Low Power"*, Kluwer,2010.
4. Kuo J.B and Lou J.H, *"Low voltage CMOS VLSI Circuits"*, Wiley 2017

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P23VLD202	EMBEDDED C++	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Explain fundamental programming concepts, including variables, conditional statements, and looping constructs.
CO2:	Apply derived data types and various types of functions (procedures) to solve programming problems.
CO3:	Demonstrate understanding of how the class mechanism supports data encapsulation and information hiding.
CO4:	Apply operator overloading and inheritance to address real-time problems in programming.
CO5:	Develop application programs for diverse peripherals and memory devices.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2	1	1	2	3
CO2	2	1	2	2	3
CO3	2	1	2	2	3
CO4	2	1	2	3	3
CO5	3	3	3	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: INTRODUCTION TO OOPS AND C++ — **9 Hours**

Object oriented concepts and its characteristics- History of C++ - Applications of C++ - Structure of C++ - Tokens — Keywords — Identifiers - Basic data types - Input and output statements - C++ Operators and control statements.

Unit 02: DERIVED DATA TYPES AND FUNCTIONS	9 Hours
Arrays - Structures - Unions - Type casting - Symbolic constants - Scope resolution operator - Functions: Function Prototyping - Function components - Passing parameters — Call by value - Call by reference - Inline function - Default arguments - Overloaded function- Introduction to friend function.	
Unit 03: CLASSES AND OBJECTS	**9 Hours**
Class specification - Member function definition - Access qualifiers - Instance creation - Static data members and member functions - Array of objects - Objects as arguments - Returning objects — Constructors - Parameterized Constructors - Overloaded Constructors - Constructors with default arguments - Copy constructors — Destructors.	
Unit 04: OPERATOR OVEROADLING AND INHERITANCE	**9 Hours**
Operator Overloading - Operator function — Overloading unary and binary operator — Inheritance Introduction — Types of Inheritance - Constructors in derived class - Abstract classes – Runtime polymorphisms - Array of pointers to base class - Virtual functions – Pure virtual functions — Virtual Destructors.	
Unit 05: PROGRAMMING ON PHERIPHERALS AND MEMORY	**9 Hours**
I/O access – Indirect I/O access – software timer – ADC -Code ROM and Data RAM – Memory management – Composition - Case study: Development of Navigation systems – Development of protocol converter.	

Theory: 45 Hrs	Tutorial: --	Practical: --	Project:--	Total Hours: 45 Hrs

REFERENCES

1.	Arkady Miasnikov, *"C++ for Embedded System"*, Independent Publishing, 6th Edition, 2015.
2.	Igor Viarheichyk, *"Embedded Programming with Modern C++ Cookbook: Practical recipes to help you build robust and secure embedded applications on Linux"*, Packt Publishing; 1st Edition, 2020..
3.	E. Balaguruswamy, *"Object-Oriented Programming with C++"*, Tata McGraw Hill, New Delhi, Sixth edition 2015.
4.	Jonathan W. Valvano ,*"Embedded Systems: Real-Time Interfacing to ARM Cortex-M Microcontrollers"*, Cengage Learning, third edition, 2019
5.	Andrew Koenig and Barbara E. Moo, "Accelerated C++: Practical Programming by Example", Addison-Wesley, 2022.

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P23VLD203	DESIGN FOR TESTABILITY	L	T	P	J	C
		2	0	0	2	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Describe testing and fault modeling.
CO2:	Analyze the test pattern generation for the combinational and sequential Circuits.
CO3:	Analyze the types of scan based testing.
CO4:	Design testable digital circuits for various applications.
CO5:	Investigate self-checking circuits.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2	1	2	3	3
CO2	2	1	2	3	3
CO3	2	1	2	3	3
CO4	2	1	2	3	3
CO5	2	1	2	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) - Theory CIE test II (10) – Theory CIE test III (10) – Theory CIE test IV(10) – Project	Assignment / Quiz/ Seminar (10) Total CIE: 50 marks Semester End Examination: 50 marks [SEE- Theory (25 marks), Project (25 marks)	Course end survey

Unit 01: BASICS OF TESTING AND FAULT MODELING — **6 Hours**

Introduction to Testing – Faults in digital circuits – Modeling of faults – Logical Fault Models – Fault detection – Fault location – Fault dominance – Logic Simulation – Types of simulation – Delay models – Gate level Event-driven simulation.

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Unit 02: TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS	6 Hours
Test generation for combinational logic circuits – Path sensitization method – Boolean Difference method – D algorithm – PODEM – Design of Testable combinational logic circuits – Reed Muller expansion technique – Three-level OR-AND-OR Design – Test generation for sequential circuits – Iterative models – State table verification – Testable design of sequential circuits.	
Unit 03: SCAN BASED DESIGNS	**6 Hours**
Controllability – Observability – Ad-hoc design – Generic scan based design – Classical scan based design – Level sensitive scan design – Clocked hazard free latches – Design rules – Advantages of LSSD – System level DFT approaches – Partial scan – Boundary scan.	
Unit 04: SELF TEST AND TEST ALGORITHMS	**6 Hours**
Test pattern generation for BIST – Exhaustive testing – Pesudorandom testing – Pseudo Exhaustive pattern generation – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.	
Unit 05: FAULT DIAGNOSIS	**6 Hours**
Diagnosis: Logical Level Diagnosis – Fault Dictionary – Guided probe testing – Diagnosis by Unit Under test reduction – Fault Diagnosis for Combinational Circuits – System Level Diagnosis. Self-checking design: Basic concepts – Application of Error detecting and error correcting codes – Multiple Bit errors – Checking circuits and parity check functions – Totally self-checking m/n code checkers - Totally self-checking Equality checkers.	
Project:	**30 Hours**
During the project work, each student focuses on fundamental skills, laying the groundwork for advanced projects that integrate theoretical knowledge with practical applications in the Design for Testability domain. Additionally, they improve their problem-solving abilities and cultivate teamwork skills essential for collaborative project development.	

Theory: 30 Hrs	Tutorial: --	Practical: --	Project: 30 Hrs	Total Hours: 60 Hrs

REFERENCES

1. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2009.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
4. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2009.
5. [illegible] "Principles of Testing Electronic Systems", John Wiley & Sons,2000

P23VLD504	CAD OF VLSI CIRCUITS	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Analyze the VLSI design methodologies and algorithmic graph theory.
CO2:	Analyze and illustrate layout design rules, placement and partitioning.
CO3:	Design and analyze floor planning and routing concept.
CO4:	Examine and verify the various modeling of simulation.
CO5:	Analyze and illustrate synthesis and scheduling.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2	1	1	2	3
CO2	2	1	2	2	3
CO3	2	1	2	2	3
CO4	2	1	2	2	3
CO5	2	1	2	2	3

Course Assessment methods		
Direct		**Indirect**
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: VLSI DESIGN METHODOLOGIES AND ALGORITHMIC GRAPHY THEORY	**9 Hours**

Introduction to VLSI Design Methodologies – VLSI Design Automation Tools – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

Unit 02: PLACEMENT AND PARTITIONING	9 Hours
Layout Compaction – Design Rules - Problem Formulation – Algorithms for Constraint Graph Compaction –Placement And Partitioning – Circuit Representation – Wire length Estimation– Placement Algorithms – Partitioning.	
Unit 03: FLOOR PLANNING AND ROUTING	**9 Hours**
Floor planning Concepts – Shape Functions and Floor Plan Sizing – Types of Local Routing Problems – Area Routing – Channel Routing – Global Routing – Algorithms for Global Routing.	
Unit 04: SIMULATION AND VERIFICATION	**9 Hours**
VLSI Simulation – Gate-Level Modeling And Simulation – Switch-Level Modeling and Simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis.	
Unit 05: HIGH LEVEL SYNTHESIS	**9 Hours**
Hardware Models for High Level Synthesis – Internal Representation of the Input Algorithm– Allocation-Assignment and Scheduling – Scheduling Algorithm – Assignment problem – High Level Transformations.	

Theory: 45 Hrs	Tutorial: --	Practical: --	Project:--	Total Hours: 45 Hrs

REFERENCES

1. Sabih H. Gerez, "Algorithms for VLSI Design Automation", Second Edition, Wiley-India, 2017.
2. Naveed A. Sherwani, "Algorithms for VLSI Physical Design Automation", 3 rd Edition, Springer, 2017.
3. Drechsler, R., *"Evolutionary Algorithms for VLSI CAD"*, Kluwer Academic publishers, Boston, 2010.
4. Hill, D., Shugard D., Fishburn J. and Keutzer K., *"Algorithms and Techniques for VLSI Layout Synthesis"*, Kluwer Academic Publishers, Boston, 2011.

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P23VLD505	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Analyze the advanced concepts of parallel processing
CO2:	Apply the memory hierarchy for multiprocessor system
CO3:	Analyze the design structures of pipelined and multiprocessor systems
CO4:	Analyze the system architecture with parallel, vector and scalable architecture for building high-performance computers
CO5:	Apply the concept of parallel processing in various architecture

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	1	1	2	3	3
CO2	1	1	2	3	3
CO3	1	1	2	3	3
CO4	1	1	2	3	3
CO5	1	1	2	3	3

Course Assessment methods		
Direct		**Indirect**
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: PARALLEL COMPUTER MODELS — 9 Hours

Multiprocessors and Multicomputers – Multivector and SIMD Computers – [illegible] Models – Conditions of Parallelism – Program Partitioning [illegible] Program Flow Mechanisms – Parallel Processing Applications – Speed Up Performance Laws

Unit 02: PROCESSOR AND MEMORY ORGANIZATION	9 Hours
Advanced Processor Technology – Superscalar and Vector Processors – Memory Hierarchy Technology – Virtual Memory Technology – Cache Memory Organization – Shared Memory Organization	
Unit 03: PIPELINE AND SUPER SCALAR TECHNIQUES	**9 Hours**
Linear Pipeline Processors – Non Linear Pipeline Processors – Instruction Pipeline Design – Arithmetic Design – Superscalar and Super Pipeline Design – Multiprocessor System Interconnects – Message Passing Mechanisms.	
Unit 04: VECTOR, MULTI THREAD AND DATAFLOW ARCHITECTURE	**9 Hours**
Vector Processing Principle – Multi-Vector Multiprocessors – Compound Vector Processing- Principles of Multithreading – Fine Grain Multi-Computers – Scalable and Multithread Architectures – Dataflow and Hybrid Architectures.	
Unit 05: SOFTWARE FOR PARALLEL PROCESSING	**9 Hours**
Parallel Programming Models – Parallel Languages and Compilers – Parallel Programming Environments Synchronization and Multiprocessing Modes – Message Passing Program Development – Mapping Programs onto Multi Computers – Multiprocessor UNIX Design Goals – MACH/OS Kernel Architecture – OSF/1 Architecture and Applications.	

Theory: 45 Hrs	Tutorial: --	Practical: --	Project:--	Total Hours: 45 Hrs

REFERENCES

1.	Kai Hwang, *"Advanced Computer Architecture"*, 3rd edition, TMH 2017.
2.	DezsoSima,TerenceFountain,PeterKacsuk,*"AdvancedComputerarchitecture –A design Space Approach"* ,Pearson Education,2 003.
3.	John P.Shen, *"Modern processor design. Fundamentals of super scalar processors"*, Tata McGraw
4.	Harry F. Jordan Gita Alaghband, *" Fundamentals of parallel Processing"*, Pearson Education , 2003
5.	Richard Y.Kain, *" Advanced computer architecture –A systems Design Approach"*, PHI, 2003

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P23VLD506	IMAGE ANALYSIS AND COMPUTER VISION	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Implement image enhancement algorithms.
CO2:	Apply image transforms for different image applications.
CO3:	Perform different segmentation and restoration
CO4:	Implement different compression techniques
CO5:	Develop algorithms for computer vision problems

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2	1	1	2	3
CO2	2	1	2	2	3
CO3	2	1	2	2	3
CO4	2	1	2	3	3
CO5	3	3	3	3	3

Course Assessment methods		
Direct		**Indirect**
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: IMAGE ENHANCEMENT

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Digital Image fundamentals - Image sampling - Quantization - Spatial domain filtering - Image negative - Contrast stretching, Gray level slicing - Histogram equalization - Smoothing filters, Sharpening filters, Maximum filter, Minimum filter, Median filter.	
Unit 02: IMAGE TRANSFORMS	**9 Hours**
2D transforms - DFT - DCT - Walsh - Hadamard - Slant - Haar - KLT - SVD - Wavelet transform.	
Unit 03: IMAGE RESTORATION AND SEGMENTATION	**9 Hours**
Image restoration - degradation model - Unconstrained and Constrained restoration - Inverse filtering - Wiener filtering - Image segmentation - Thresholding - Edge detection - Region based segmentation.	
Unit 04: IMAGE COMPRESSION	**9 Hours**
Need for data compression - Huffman - Arithmetic coding - LZW technique - Vector Quantization - JPEG – MPEG	
Unit 05: COMPUTER VISION	**9 Hours**
Texture classification - Feature extension - Markov Random Field Matrix – Gray Level Co – occurrence Matrix – Gray Level Weight Matrix , Multi Resolution Combined Statistical and Spatial Frequency method, character recognition- zoning approaches, Medical Image Analysis – Diabetic Retinopathy – Glaucoma.	

Theory: 45 Hrs	Tutorial: --	Practical: --	Project:--	Total Hours: 45 Hrs

REFERENCES

1.	Rafael C.Gonzalex, Richard E.Woods, *"Digital Image Processing, Pearson Education. Inc"*., Forth Edition, 2018.
2.	Anil K.Jain, *"Fundamentals of Digital Image Processing"*, Prentice Hall of India, 2004.
3.	Milan Sonka, Vaclav Hlavac and Roger Boyle, *"Image Procesing, Analysis and Machine Vision"*, Brookes/Cole, Vikas Publishing House, 2nd edition, 1999.
4.	Jayaraman S Esakkirajan and Veerakumar, "Digital Image Processing", McGraw Hill Education; July 2017
5.	Sid Ahmed, M.A., *"Image Processing Theory, Algorithms and Architectures"*, Mc Graw Hill, 1995.

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P23VLD204	VLSI DESIGN AND TESTING LABORATORY	L	T	P	J	C
		0	0	2	0	1

Course Outcomes

At the end of the course, the student will be able to

CO1:	Design and simulate the performance analysis of source followers, and OP- AMPs
CO2:	Design and simulate test and verification using system Verilog
CO3:	Implementation of the real time application using FPGA

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2	1	3	3	2
CO2	2	1	3	3	2
CO3	2	1	3	3	2

Course Assessment methods

Direct		Indirect
CIE test I (20) Quiz 1 (5) CIE test II (20) Quiz 2 (5)	RTPS (10) Total CIE: **60 marks** Semester End Examination: **40 marks**	Course end survey

List of Experiments

1. Analog circuits case studies - Schematic entry to GDS II layout
   Design and simulate frequency response and noise analysis of any Source followers
2. Design and simulate operational amplifier performance parameters - One-stage Op Amps, Two-stage Op Amps
3. Design and implement FIR and IIR filters
4. Design and implement LMS adaptive filters
5. Verification of combinational circuits using system Verilog
6. Verification of sequential circuits using system Verilog
7. Implementation of Elevator controller using FPGA
8. Implementation of Model Train controller using FPGA

Theory: 0	Tutorial: 0	Practical: 30 Hrs	Project: 0	Total Hrs: 30 Hrs

27/1/25

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P23VLD205	MINI PROJECT	L	T	P	J	C
		0	0	0	2	1

Course Outcomes

At the end of the course, the student will be able to

CO1:	Identify the thrust areas in VLSI and related domains.
CO2:	Formulate the methodology in interdisciplinary mode.
CO3:	Draft the methodology and develop the product/algorithm related to VLSI domain.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	3	3
CO2	3	3	3	3	3
CO3	3	3	3	3	3

Course Assessment methods

Direct		Indirect
Review I - 5 Marks Review II -10 Marks Review III-15 Marks Final Project Report- 10 Marks	Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

This mini-project course provides students with an opportunity to apply the knowledge and skills acquired in the Master of Engineering (ME) program in VLSI Design to a practical design project. Through hands-on experience, students will gain proficiency in various aspects of VLSI design, including design methodologies, simulation, layout, and verification.

Theory: 0	Tutorial: 0	Practical: 0	Project: 30 Hrs	Total Hours: 30 Hrs

27/1/25

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P23GE701	English for Research Paper Writing	L	T	P	J	C
		2	0	0	0	0

Course Outcomes

At the end of the course, the student will be able to

CO1:	Demonstrate research writing skills both for research articles and thesis
CO2:	Frame suitable title and captions as sub-headings for articles and thesis
CO3:	Write each section in a research paper and thesis coherently
CO4:	Use language appropriately and proficiently for effective written communication
CO5:	Exhibit professional proof-reading skills to make the writing error free

Course Assessment methods

Direct		Indirect
CIE test I (30) CIE test II (30) CIE test III (40)	Total CIE: 100 marks Semester End Examination: NIL	Course end survey

Unit 01:	**6 Hours**
Planning and preparation, word order, breaking up long sentences, organising ideas into paragraphs and sentences, being concise and avoiding redundancy, ambiguity and vagueness	
Unit 02:	**6 Hours**
Interpreting research findings, understanding and avoiding plagiarism, paraphrasing sections of a paper/ abstract.	
Unit 03:	**6 Hours**
Key skills to frame a title, to draft an abstract, to give an introduction	
Unit 04:	**6 Hours**
Skills required to organise review of literature, methods, results, discussion and conclusions	
Unit 05:	**6 Hours**
Usage of appropriate phrases and key terms to make the writing effective - proof-reading to ensure error-free writing	

Theory: 30 Hrs	Tutorial: --	Practical: --	Project:--	Total Hours: 30 Hrs

TEXT BOOKS

1.	Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2.	Highman N , Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book, 1998
3.	Day R, How to Write and Publish a Scientific Paper, Cambridge University Press, 2006.
4.	Goldbort R, Writing for Science, Yale University Press, 2006. (available on Google Books)

REFERENCES

1	Martin Cutts, Oxford Guide to Plain English, Oxford University Press, Second Edition, 2006

HOD

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Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for M.E/M.Tech. Semester III under Regulations 2023 (CBCS)
Branch: VLSI Design

S.No	Course Code	Course Title	L	T	P	J	C	Category	Total Contact Hours	Course Type*
Theory courses										
1.	**P23VLD503**	**Elective:** ASIC Design	3	0	0	0	3	PE	45	T
2.	**P23VLD507**	**Elective:** Nano Electronics	3	0	0	0	3	PE	45	T
3.	**P23VLD516**	**Elective:** Analysis and Design of Digital Integrated Circuits	3	0	0	0	3	PE	45	T
4.	**P23VLD301**	Project Work-I	0	0	0	16	8	PC	240	P
Total Credits							**17**			

*T- Theory, TT- Theory with Tutorial, TL- Theory with Laboratory, TP- Theory with Project, TLP- Theory with Laboratory and Project, L-Laboratory, LT- Laboratory with Theory, LP- Laboratory with Project ,P-Project

Approved By

14/6/25	20/6/25	20/6/25	
Chairperson – ECE BoS	**Member Secretary/ Academic Council**	**Dean-Academics**	**Chairperson, Academic Council & Principal**
Dr.R.S.Sabeenian	**Dr.R.Shivakumar**	**Dr.J.Akilandeswari**	**Dr.S.R.R.Senthil Kumar**

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Copy to:
HOD/ ECE, Third Semester ME VLSI Students and Staff, COE

P23VLD503	ASIC DESIGN	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Apply Logical Effort Technique for predicting Delay, Delay Minimization and FPGA Architectures.
CO2:	Analyze and design the programmable ASIC Architecture.
CO3:	Design Logic Cells and I/O Cells.
CO4:	Use Algorithms for Floor Planning and Placement of Cells and to Apply Routing Algorithms for Optimization of Length and Speed.
CO5:	Analyze High Performance Algorithms Available for ASICs.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2		3	3	3
CO2	2		3	3	3
CO3	2		3	3	3
CO4	2		3	3	3
CO5	2		3	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01: INTRODUCTION TO ASIC CMOS LOGIC AND ASIC LIBRARY DESIGN	9 Hours

Types of ASICs – Design Flow – CMOS Transistors CMOS Design Rules – Combinational Logic Cell – Sequential Logic Cell – Data Path Logic Cell – Transistors As Resistors - Transistor Parasitic Capacitance– Logical Effort –Library Cell Design - Library Architecture

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Unit 02 : PROGRAMMABLE ASIC ARCHITECTURE	9 Hours
Architecture and configuration of ARTIX - STRATIX FPGA - Zynq FPGAs – Micro-Blaze - Nios based embedded systems – Signal probing techniques	
Unit 03 : PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS	**9 Hours**
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC and AC inputs and outputs - Clock and Power inputs - Xilinx I/O blocks	
Unit 04 : LOGIC SYNTHESIS PLACEMENT AND ROUTING	**9 Hours**
Logic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning - Floor Planning Tools - I/O and Power Planning - Clock Planning - Placement Algorithms - Routing: Global Routing - Detailed Routing - Special Routing	
Unit 05 : HIGH PERFORMANCE ALGORITHMS FOR ASICS SOCS AND SOC CASE STUDIES	**9 Hours**
SoC Design Flow- Platform-Based and IP Based SoC Designs - Basic Concepts of Bus-Based Communication Architectures - High performance filters using delta-sigma modulators- Case Studies: Digital camera - SDRAM- High speed data standards	

Theory: 45 Hrs	Tutorial: 0Hrs	Practical: 0	Project: 0	Total Hours: 45 Hrs

REFERENCES

1. Smith M.J.S, "Application Specific Integrated Circuits", Addison -Wesley Longman Inc, 2011.
2. Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, "FPGA-Based Implementation of Signal Processing Systems", Wiley, 2008.
3. Steve Kilts, "Advanced FPGA Design," Wiley Inter-Science,2006.
4. Wayne Wolf., "Modern VLSI Design System-On –Chip Design", Pearson Education, 2005.
5. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.

Prepared By
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P23VLD507	NANO ELECTRONICS	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Design and illustrate circuit design using FINFET.
CO2:	Design SRAM, NRAM, MRAM and NATURE.
CO3:	Design nano-wire and NASIC circuits.
CO4:	Analyze CNT and design FPCNA.
CO5:	Design the circuit using grapheme transistor, RTD and QCA.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	1	1	2	3	3
CO2	1	1	2	3	3
CO3	1	1	2	3	3
CO4	1	1	2	3	3
CO5	1	1	2	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 01	FINFET CIRCUIT DESIGN	9
	Introduction of FinFETs – Shorted-Gate and Independent-Gate FinFETs – Logic Design using FinFETs – Threshold Voltage Control through Multiple Supply Voltages – The Principle of TCMS – Logic Design using TCMS – Schmitt Trigger using FinFETs– Latch Design using FinFETs – Precharge – Evaluate Logic Circuits using FinFETs – FinFET Layout – Oriented FinFETs.	
Unit 02	**HYBRID NANO CMOS IN SRAM**	**9**
	Fundamentals Nonplanar SRAM–Modeling of FinFET Devices for SRAM Applications– SRAM Design–Finfet Design for SRAM – NRAM – MRAM – PCM– Temporal Logic Folding–Architecture of Nature – Power Estimation–Nanomap Optimization Flow.	

14/6/2025

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Unit 03	CHARACTERIZATION TECHNIQUES, NANO WIRE ARRAYS AND NANOSCALE ASIC	9
	Nano wires Fabrication Technologies – Crossbar Technologies– Architecture of Nanowire Crossbars-Testing Crossbars-NASIC Building Blocks – NASIC Circuit Styles – NASIC Logic Styles – NASIC Architectures – Nano sensors.	
Unit 4	CARBON NANOTUBE VLSI CIRCUITS AND FPCNA	9
	CNTFET– Mis Positioned-CNT – Immune Logic Design – Design-Metallic CNT Immune CNFET Circuits – VLSI Compatible Metallic – CNT Removal – Design Flow – Nano electronic Devices – FPCNA Architecture –Nanotube LUT Fabrication.	
Unit 5	GRAPHENE TRANSISTOR, RTD AND QUANTUM CELLULAR AUTOMATE	9
	Fabrication – Graphene Tansistors–Analog Circuits –Digital Circuits – Resonant Tunneling Diodes Fundamentals – QCA Fundamentals – Logic Design With QCA.	

Theory: 45 Hrs	Tutorial: 0 Hrs	Practical: 0	Project: 0	Total Hours: 45 Hrs

REFERENCES

1. Deming Chen and Niraj K. Jha., *"Nanoelectronic Circuit Design"*, Springer, 2014.
2. Nladimir V. Mitin,Viatcheslav A. Kochelap& Michael A. Stroscio., *"Introduction to Nanoelectronics Science, Nanotechnology, Engineering and Applications"*, Cambridge University Press, 2012.
3. Peter J.F. Harris, *"Carbon Nanotube Science Synthesis, Properties and Applications"*, Cambridge University Press, 2011.
4. Hanson, Fundamentals of Nanoelectronics, Pearson education, 2009.
5. Goser K., Glosekotter P. Dienstuhl J., *"Nanoelectronics and Nanosystems from Transistors to molecular and quantum Devices"*, Springer, 2008.

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P23VLD516	ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS	L	T	P	J	C
		3	0	0	0	3

Course Outcomes

At the end of the course, the student will be able to

CO1:	Explain the digital integrated circuits design and its fabrication simulation.
CO2:	Analyze the MOS inverter circuits and static MOS gate circuits.
CO3:	Analyze the high speed CMOS logic design, transfer gate and dynamic logic design.
CO4:	Discuss about the semiconductor memory design.
CO5:	Examine the interconnect, power grid and clock design.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	2	1	2	3	3
CO2	2	1	2	3	3
CO3	2	1	2	3	3
CO4	2	1	2	3	3
CO5	2	1	2	3	3

Course Assessment methods

Direct		Indirect
CIE test I (10) CIE test II (10) CIE test III (10)	Assignment / Problem-solving / Seminar (10) Total CIE: **40 marks** Semester End Examination: **60 marks**	Course end survey

Unit 1	DEEP SUBMICRON DIGITAL IC DESIGN AND MOS TRANSISTORS	9
	Review of Digital Logic Gate Design – Digital IC design – Computer aided design of Digital circuits. The MOS transistor – Structure and operation of MOS transistor. Bipolar Transistor and Circuit -IC fabrication technology – Layout basics – Modeling the MOS transistor for circuit simulation – SPICE MOS level-1 device model – BSIM3 model – SOI technology.	

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Unit 2	MOS INVERTER CIRCUITS AND STATIC MOS GATE CIRC	9
	Voltage transfer characteristics – Noise margin definitions –Resistive load inverters – NMOS transistor as load devices – Complementary MOS inverters – Pseudo NMOS inverters – Sizing inverters – Tristate inverters. CMOS gate circuits.	
Unit 3	HIGH SPEED CMOS LOGIC DESIGN, TRANSFER GATE AND DYNAMIC LOGIC DESIGN	9
	Switching time analysis – Detailed load capacitance calculation – Improving delay calculation with input slope – gate sizing for optimal path delay – optimizing path with logical effort. Basic concepts of transfer gate – CMOS transmission gate logic – Dynamic D latches and D flip flops-Domino Logic-Voltage Bootstrapping.	
Unit 4	SEMICONDUCTOR MEMORY DESIGN	9
	Introduction – MOS decoders – Static RAM cell design – SRAM column I/O circuitry – Memory architecture. Content addressable memories – FPGA – Dynamic read – write memories – Read only memories – EPROMs and EEPROMs – Flash memory – FRAMs	
Unit 5	INTERCONNECT, POWER GRID AND CLOCK DESI	9
	Interconnect RC delays – Buffer insertion for Very long wires – Interconnect coupling capacitance – interconnect inductance – antenna effects. Power distribution design – clocking and timing issues – Phase locked loops/delay locked loops.	

Theory: 45 Hrs	Tutorial: 0Hrs	Practical: 0	Project: 0	Total Hours: 45 Hrs

REFERENCES	
1.	David A Hodges, Horace G Jackson, Resve A Saleh, "Analysis And Design Of Digital Integrated circuits – in deep submicron technology", Tata McGraw Hill, Third Edition 2003.
2.	Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated circuits Analysis and Design, Tata McGraw Hill, Third Edition 2002.

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P23VLD301	PROJECT WORK-I	L	T	P	J	C
		0	0	0	16	8

Course Outcomes

At the end of the course, the student will be able to

CO1:	Identify the thrust areas in VLSI and related domains.
CO2:	Formulate the methodology in interdisciplinary mode.
CO3:	Draft the methodology and develop the product/algorithm related to VLSI domain.

Pre-requisite:

CO/PO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Program Outcomes (POs)				
	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	3	3
CO2	3	3	3	3	3
CO3	3	3	3	3	3
CO4	3	3	3	3	3
CO5	3	3	3	3	3

Course Assessment methods

Direct		Indirect
Review I - 5 Marks Review II - 10 Marks Review III- 15 Marks Final Project Report- 10 Marks	Total CIE: **40 marks** Semester End Examination : **60 Marks**	Course end survey

- Every project may hold one faculty member appointed by the HOD as a supervisor who is expert in the domain chosen by the team.
- The project problem formulated should be innovative and unique in ECE domain.
- Final solution identified by the student may be converted in to prototype.
- The hours allotted for this course shall be utilized by the students to receive directions from the supervisor to refer the existing literatures and perform the experiments in the lab to come up with the low cost solutions.
- Periodic reviews shall be held by the expert committee identified by the Head of the Department and assessment may be done.
- Monitoring committee may be appointed to regularly monitor the progress work of the student team.
- Final report and relevant documents to be submitted and final assessment will be done by the internal and external examiners appointed by the COE.

Theory: 0	Tutorial: 0	Practical: 0	Project: 240 Hrs	Total Hours: 240 Hrs

Prepared By
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14/6/2025
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Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for M.E/M.Tech. Semester IV under Regulations 2023 (CBCS)
Branch: VLSI Design

S.No	Course Code	Course Title	L	T	P	J	C	Category	Total Contact Hours	Course Type*
Practical courses										
1.	P23VLD401	Project Work-II	0	0	0	28	14	PC	420	P
						Total Credits	**14**			

*T- Theory, TT- Theory with Tutorial, TL- Theory with Laboratory, TP- Theory with Project, TLP- Theory with Laboratory and Project, L-Laboratory, LT- Laboratory with Theory, LP- Laboratory with Project

Approved By

12/12/2025			
Chairperson, Electronics and Communication Engineering BoS	**Member Secretary, Academic Council**	**Dean-Academics**	**Chairperson, Academic Council & Principal**
Dr.R.S.Sabeenian	**Dr.R.Shivakumar**	**Dr.J.Akilandeswari**	**Dr.S.R.R.Senthil Kumar**

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Copy to:-
HOD/ Electronics and Communication Engineering, Fourth Semester M.E VLSI Students and Staff, COE

P23VLD401	PROJECT WORK-II	L	T	P	J	C
		0	0	0	28	14

Course Outcomes

At the end of the course, the student will be able to

CO1:	Identify problems, formulate literature survey, and analyse problems related to VLSI Design in multidisciplinary areas.
CO2:	Design and conduct experiments to interpret data pertaining to VLSI Domain.
CO3:	Prepare documentation and presentation.

Pre-requisite: ---

CO/PO, PSO Mapping

(3/2/1 indicates the strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcomes (PSOs)				
	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	3	3
CO2	3	3	3	3	3
CO3	3	3	3	3	3

Course Assessment methods

Direct		Indirect
Review I - 5 Marks Review II -10 Marks Review III-15 Marks Final Project Report- 10 Marks	Total CIE: 40 marks Semester End Examination: (60)	Course end survey

Project work instructions:

- Every project may hold one faculty member appointed by the HOD as a supervisor who is expert in the domain chosen by the team.
- The project problem formulated should be innovative and unique in VLSI domain.
- Final solution identified by the student may be converted in to prototype.
- The hours allotted for this course shall be utilized by the students to receive directions from the supervisor to refer the existing literatures and perform the experiments in the lab to come up with the low cost solutions.
- Periodic reviews shall be held by the expert committee identified by the Head of the Department and assessment may be done.
- Monitoring committee may be appointed to regularly monitor the progress work of the student team.
- Final report and relevant documents to be submitted and final assessment will be done by the internal and external examiners appointed by the COE.

Theory: -	Tutorial: -	Practical: --	Project:420Hrs	Total Hours: 420 Hrs

12/12/24
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